

**University of Pennsylvania**  
**Department of Electrical and System Engineering**  
**Computer Organization**

ESE534, Spring 2012

Assignment 8: Rent's Rule

Monday, Mar. 19

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**Due:** Monday, March 26, 12:00PM

1. For HW6.2 (LUT Design):
  - (a) Decompose your design recursively into subtrees (like problem 1 on preclass Day 16). Show mapping of individual LUTs to tree leaves and the number of signals on each channel edge in the tree. Leaf of the tree is the 5-LUT (including the cascade input); that is, treat the cascade input like any other input for this problem. Since you are not using the flip-flop, the output of the LUT and the cascade output are the same signal, so treat them as such.
  - (b) Compute maximum IO's at each tree level.
  - (c) Estimate Rent parameters ( $c$ ,  $p$ ) from your answer to part (b).
  - (d) Show layout of the design on a  $c = 6$ ,  $p = 0.5$  tree. This may require re-association and LUT depopulation to fit on the wire schedule of the tree. Circuit IO's should come through the root of the tree.
  
2. Estimate wire minimizing cuts and record the IO vs. capacity ratios for the following. Estimate the associated Rent parameters ( $c$  and  $p$ ).
  - (a) Unbanked memory (HW7.1)  $N = d = w = 2^{10}$
  - (b) Banked memory (HW7.2)  $N = 2^{10}$ ,  $d = 2^5$ ,  $b = 2^5$ ,  $w = 2^5$  then  $2^5$  of these in parallel to make up  $w_{total} = 2^{10}$  (so total capacity and width ends up being the same as (a) – but internal organization is different).
  - (c)  $64 \times 64$  simple array multiplier (HW2.1)
  - (d)  $64 \times 64$  associative reduce multiplier (HW2.3)

3. What does Rent's Rule tell us (not tell us) about the dynamic switching energy requirements for a computation? Assume:
- $E = \sum_{\text{all nets } i} \left( \frac{1}{2} a_i C_i V^2 \right)$
  - Voltage is fixed.
  - activity factor,  $a_i$  varies per net.
  - net capacitance,  $C_i$ , will include capacitance from all the wires on the net.
  - $C_{\text{wire}}$  is proportional to its length.
- (a) Given the  $N$ ,  $c$ ,  $p$  for a design, give bounds on the energy requirement. [State assumptions as necessary. You will likely need to make several.]
- (b) The bisections for Rent calculation do not take into account the activity factor,  $a$ .
- i. Describe how this effects the accuracy of a Rent-only estimate of energy?
  - ii. Describe how you might define and obtain a better estimate of interconnect energy that follows the spirit of the Rent estimate, but takes into account knowledge of activity factors. [open ended question]
4. What is the energy impact of mismatched wire schedules for spatially configured computations (*e.g.* FPGAs – instructions do not change from cycle-to-cycle) using the homogeneous Tree-of-Meshes design from Day 16. Make the simplifying assumption of uniform activity factors on *used* nets for this question; assume unused wires do not switch. Assume wire dominated and think about wire lengths.
- (a) What is the energy efficiency of a mismatch mapping where  $c_{\text{design}}, p_{\text{design}}$  is larger than  $c_{\text{net}}, p_{\text{net}}$ ? (You may assume the simple case where you use a suitable power-of-2 larger tree and you “pull the design up” to the tree to meet the required wire schedule.)
- (b) What is the energy efficiency of a mismatch mapping where  $c_{\text{design}}, p_{\text{design}}$  is smaller than  $c_{\text{net}}, p_{\text{net}}$ ?