University of Pennsylvania
Department of Electrical and Systems Engineering
Electronic Design Automation

ESE535, Spring 2008 Assignment #1 Wednesday, January 23

Due: Monday, February, 4th, beginning of class.

Resources You are free to use any books, articles, notes, or papers as references. Provide citations in your writeup as appropriate.

Collaboration Please work independently on this assignment.

Writeup Writeup should be in an electronically readable format (HTML or PDF preferred—I do not want to decipher handwriting or hand-drawn figures). State any assumptions you need to make.

Energy Model For this assignment we'll use a simple energy model. We lump all capacitance for the nodes to the LUT input and assume this is the same for all LUTs (so this ignores effects of wire lengths, just as the unit delay assumption does). We assume the dominant energy is the energy taken to switch each of these inputs. The energy is thus:

$$E_{circuit} \propto \sum_{\text{all gate inputs}} (P_{switch}(\text{input}))$$

For covering, assume the input netlist is already annotated with the switching probability of each gate. Particularly, gate inputs in the input netlist which are hidden inside a mapped gate during covering do **not** contribute to the energy for the mapped circuit.

Problems

1. Show an example where all three optimization criteria would give rise to different optimal coverings:
   - area (in LUTs)
   - delay (in LUT delays; you may assume fanout does not affect delay)
   - energy (as described above; you may assign switching probabilities to the gate inputs in the input netlist as you need to construct your example)
2. In LUT covering/clustering for energy minimization, does exposed switching activity have a monotone property? Explain why or why not.

3. The following helps underscore why area optimization (even under the duplication-free restriction) is more complicated than delay mapping. You may want to take a look at [1].

   (a) Show an example where the mincut from a target node is 3 but the best cut to use for k=4-LUT area minimization is of size 4.

   (b) Give the trivial $O(n^{k+1})$ algorithm for exploring all k-feasible cuts. ([1] gives a more complicated algorithm which is significantly faster in practice.)

4. Develop a dynamic-programming based algorithm for LUT covering to minimize energy consumption (based on the model given above).

   (a) Give pseudocode for your algorithm in the style of [1] or [2].

   (b) Analyze the complexity/running time of your algorithm.

   (c) Explain the optimality of your solution (for what classes of problems is it optimal? in what cases is it non-optimal and why?).

References

[1] Jason Cong and Yuzheng Ding. On area/depth trade-off in lut-based fpga technology mapping. *IEEE Transactions on VLSI Design*, 2(2):137–148, June 1994.

[2] Thomas Cormen, Charles Leiserson, and Ronald Rivest. *Introduction to Algorithms*. MIT Press, 1990.