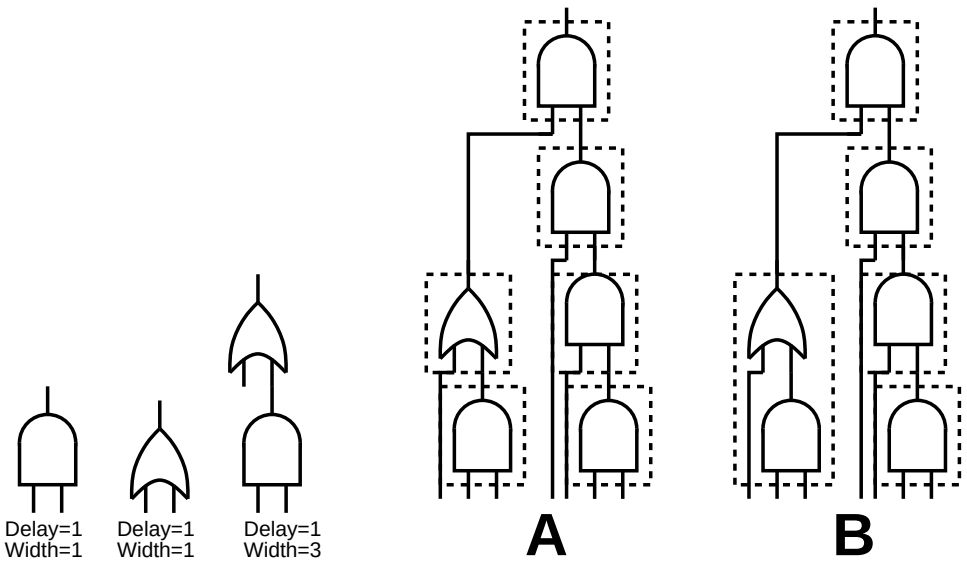
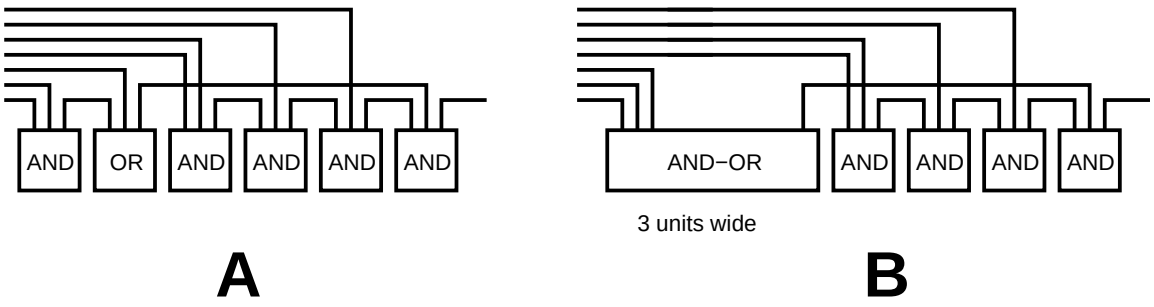
Consider the following covers.



1. What is the delay for each of the two covers?

A ☐ B ☐

2. Consider the following 1D layouts for these two covers. What is the delay for each cover assuming 0.5 units of delay for each unit cell width the wire travels?



A ☐ B ☐