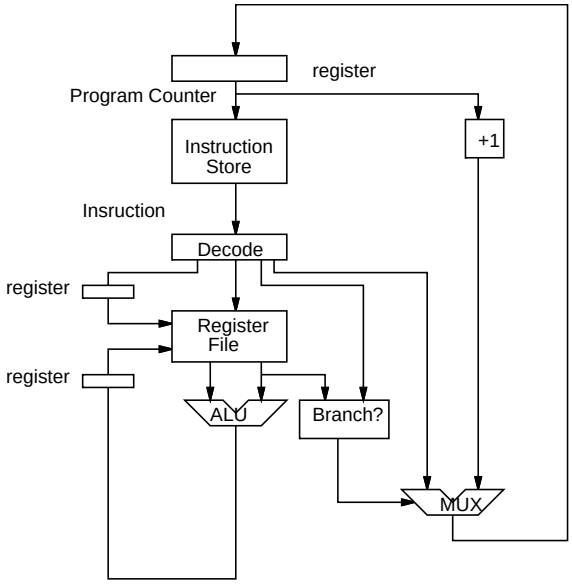
Consider the following simple processor:



Assume:

- Writes occurring on the same cycle as reads appear to happen before the read (*i.e.*, the read gets the newly written value).
- Program Counter is 16 bits wide.
- Register File and ALU are 16 bits wide.
- There are 8 registers (R0, R1,...R7).
- Instruction store is not writable (you may consider it a ROM).

Questions:

1. How many total bits representing state? ☐
2. How many states does the processor have? ☐
3. Assume the design is further pipelined between each of the major stages (instruction fetch, register access, ALU operation); appropriate bypass and interlock logic is added.
   (a) Estimate a lower bound on the number of additional state bits. ☐
   (b) With these additional state bits, how many total states does the pipelined processor have? ☐