

University of Pennsylvania
Department of Electrical and Systems Engineering
Electronic Design Automation

ESE535, Spring 2009

Assignment #5

Wednesday, April 8

Due: Wednesday, April 22, beginning of class.

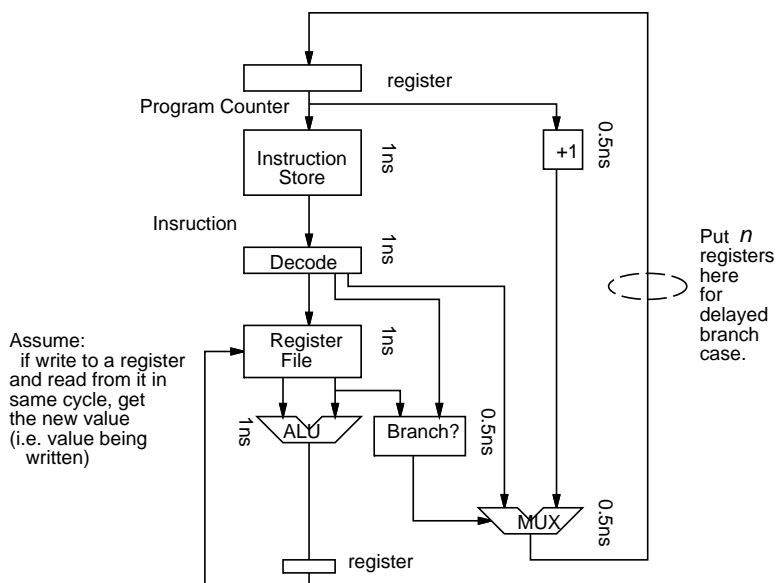
Resources: You are free to use any books, articles, notes, or papers as references. Provide citations in your writeup as appropriate.

Collaboration: Please work independently on this assignment. For problem 2 only, you may discuss general algorithmic strategies and help each other with the compiler, build environment, and debugging, but each student should develop his or her own solution. If you do discuss strategy or get debugging help, please acknowledge in your writeup.

Writeup: Writeup should be in an electronically readable format (HTML or PDF preferred—I do not want to decipher handwriting or hand-drawn figures). State any assumptions you need to make.

Problem 1 (offline) [3pts]

Consider the following, simple microcontroller datapath:



1. What is the delay of the datapath as shown?

Consider changing the branch instruction to a delayed branch instruction that transfers control n cycles after the branch is issued. This is equivalent to putting n registers on the path as shown.

2. Using the retiming procedure from class:
 - (a) How does the clock cycle change with n ?
 - (b) Above what value of n does further increase of n result in no further decrease in cycle time? Why? (Show the $G-1/C$ graph and use that in your explanation.)
 - (c) For this maximum useful value of n , show the retimed circuit that achieves the minimum cycle time.
3. Starting from the retimed circuit with the maximum useful branch delay, n . C -slow the circuit so that the cycle time of the C -slowed circuit is equal to the delay of the ALU.
 - (a) What is the value of C necessary to achieve this?
 - (b) Show the circuit after C -slowing and retiming the circuit. Color each of the C different register sets differently similar to the example in the Day 18 lecture.

[Note: This is a deliberately simple datapath. While processors did go through a period where they used delayed branches, that was ultimately considered a poor idea for technology-abstract ISA scalability. Modern processors use many more techniques to deal with this cyclic dependence, but some do run interleaved streams using a similar idea to C -slowing. For more details see CIS501.]

Problem 2 (programming) [7pts]

Develop a routine to perform one-dimensional placement to minimize channel width on graphs in the format we have used for previous assignments. That is, we assume we can implement each of the operators (*e.g.* Add, Multiply) as a slice of a fixed width and assemble these end-to-end. Our key freedom is the ordering of the operators in the datapath. For this assignment, the Input and Output blocks represent memory banks that supply inputs and store results, respectively.

Two layouts for a simple datapath are shown below:



Provided starting point is available in `~ese535/spring2009/assign5.tar` on `eniac`. This uses similar building blocks as previous assignments. Put your routine in `your_place.c`.

Note that there are routines in `placement.c` for placing nodes and computing channel width. The `channel_width` function is a relatively expensive calculation (possibly $O(N^2)$), so you should not use it in the inner loop of your optimization routine. Hint: would you want to use it even if it were cheaper to calculate?

The benchmark set is a subset of the benchmarks you have been using in previous assignments.

Turnin:

1. Your code (a tar file as on previous assignments that can be unpacked and built)
2. A description of your placement strategy including cost function(s) used and rationale for selection.
3. Summary of your results across the provided benchmark set including:
 - channel width before your placement routine
 - channel width after your placement routine
 - percentage improvement
 - runtime for your placement routine