

University of Pennsylvania
Department of Electrical and Systems Engineering
Electronic Design Automation

ESE535, Spring 2009

Assignment #6

Monday, April 20

Due: Tuesday, May 12, 12PM (noon).

Resources: You are free to use any books, articles, notes, or papers as references. Provide citations in your writeup as appropriate.

Collaboration: Please, work independently on this assignment.

Writeup: Writeup should be in an electronically readable format (HTML or PDF preferred—I do not want to decipher handwriting or hand-drawn figures). State any assumptions you need to make.

1. [2pts] Consider the following two-sided channel routing problem:

top	1	nc	nc	3	2	1	3	4	1	2	3	nc	4	5
bottom	nc	2	1	3	4	2	5	5	nc	4	3	4	1	nc

nc = no connection

Assume you have two layers of metal for routing.

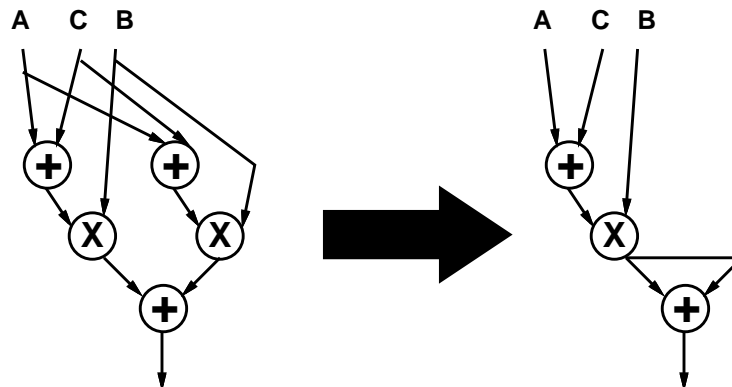
- Draw the vertical constrain graph (VCG)
 - Resolve any conflicts which the VCG highlights; show the revised problem.
 - Route the channel, minimizing the number of tracks; show the resulting channel with track routing.
 - Compare the achieved channel width to the channel density lower bound.
2. Consider a variation where there was an additional vertical pin position with connections neither on the top or bottom as shown below:

top	1	nc	nc	3	2	1	3	4	1	2	3	nc	nc	4	5
bottom	nc	2	1	3	4	2	5	5	nc	4	3	4	nc	1	nc

[1pt] How would you change the route to exploit the extra vertical pin position and achieve the channel density lower bound?

3. [2pt] Completely describe an algorithm for channel routing that exploits this additional freedom (*i.e.* using available vertical segments for dogleg track jogs to minimize channel width). You may want to consider how the negotiated congestion techniques in Pathfinder could be applied here, but you are not required to use those techniques in your solution. If you use a Pathfinder-like solution, you will need to describe the routing graph you use to represent the channel routing problem. Your solution should be time efficient (*i.e.* avoid exponential-time algorithms).

4. Consider the simple example circuit we used to illustrate common subexpression elimination (CSE) in assignment 4 and its optimized result.



Assume that the probability distribution function (PDF) for the delay of the two operators can be approximated as follows:

Add	delay	180ps	200ps	
	P(delay)	0.2	0.8	
Multiply	delay	900ps	1000ps	1100ps
	P(delay)	0.05	0.6	0.35

[1pt] Give the PDF for the complete circuit delay for the circuit both before and after CSE.

5. [4pt] Provide an improved algorithm for placement and routing of standard cell gates. Standard cells are designed to a common fixed height, with gate-specific widths. Inputs and outputs are available on both sides of the cell as illustrated in class.

As a strawman starting point, consider a flow that performed:

- Use 2D Placement of gates using simulated annealing to minimizing squared wire length.
- Rows of the 2D placement become standard-cell rows.
- Add a set of vertical route blocks to provide vertical interconnect among rows. These are added incrementally in greedy fashion. That is each vertical route block between existing cells and vertical route blocks is placed in a position that will minimize the squared wire length. That is, for a net_n , we select an x_{rt} to minimize:

$$\sum_{j=y_{min}(net_n)}^{y_{max}(net_n)} (\max(x_{max}(j, net_n), x_{rt}) - \min(x_{min}(j, net_n), x_{rt}))^2$$

where $y_{min}(net_n)$ and $y_{max}(net_n)$ are the minimum and maximum channel where net_n needs to appear, and $x_{max}(j, net_n)$ and $x_{min}(j, net_n)$ define the largest and smallest x position of net net_n in channel j . When x_{rt} falls in the middle of a cell, the vertical route through is placed to one side of the standard cell so as to minimizing its displacement from the ideal x_{rt} position.

- Use constrained Left-Edge algorithm to channel route within each channel.

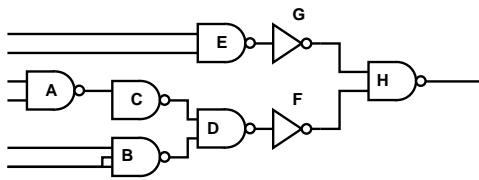
An example is shown on the following page.

We know from class and Problem 1 that vertical constraints in the channel may increase channel width beyond the channel density. The simple 2D, squared-wirelength-minimizing simulated-annealing placement does nothing to avoid or reduce vertical constraints, nor does the technique described for inserting vertical route blocks.

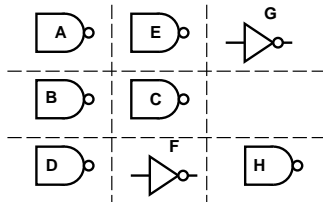
- (a) What other weaknesses does this strawman flow have?
- (b) Your task is to improve this placement and routing flow. You are encouraged to consider any and all of:
 - adding new moves or transformations
 - changing optimization cost functions
 - replacing optimization steps
 - inserting additional optimization steps
 - changing the sequence of operations, including iterating operations

Your final description should be complete and stand-alone. That means you will need to fully define moves, cost functions, and cooling schedules (if appropriate).

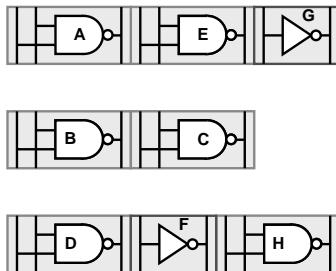
Netlist



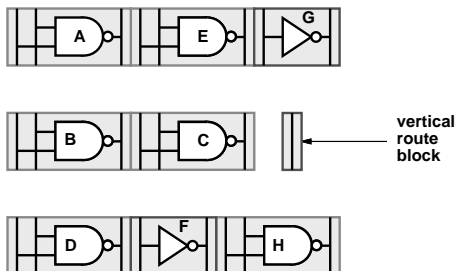
2D Place



Standard Cell Rows



Add Vertical Route Blocks



Route Channels

