Assume you have N 2-input NAND gates placed in a $\sqrt{N} \times \sqrt{N}$ array. Assume each gate is of size $L_g \times L_g$. Track width, W, between the rows and columns will be adjusted to be just large enough to route the wires needed to interconnect the gates.

1. How wide is the channel-width W if all gates get their 2 inputs from their North and West neighbors?

$$W = \square$$

2. How wide is the channel-width W if all gates get their 2 inputs from the opposite quadrant of the chip (*i.e.* cells in the NE quadrant get inputs from the SW quadrant (and vice-versa) and cells in the SE quandrant get inputs from the NW quadrant) ?

$$W = \square$$

3. Assuming wires have finite width L_w and the chip has one horizontal and one vertical routing layer, what is the area of the chip in each of the two cases above?

$$A_{pr1} = \square$$

$$A_{pr2} = \square$$

4. Keeping the same wiring assumptions, what is the length of the wires in the two cases above?

$$L_{pr1} = \square$$

$$L_{pr2} = \square$$