

ESE535: Electronic Design Automation

Day 3: January 26, 2009
Scheduled Operator Sharing



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Last Time

- How to construct a dataflow graph from a high-level language
 - From C

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Today

- Sharing Resources
- Area-Time Tradeoffs
- Throughput vs. Latency
- VLIW Architectures

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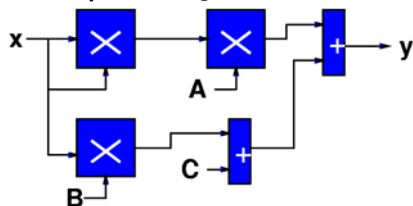
Compute Function

- Compute:
$$y = Ax^2 + Bx + C$$
- Assume
 - $D(\text{Mpy}) > D(\text{Add})$
 - $A(\text{Mpy}) > A(\text{Add})$

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Spatial Quadratic



- $A(\text{Quad}) = 3 \cdot A(\text{Mpy}) + 2 \cdot A(\text{Add})$

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Latency vs. Throughput

- **Latency:** Delay from inputs to output(s)
- **Throughput:** Rate at which can introduce new set of inputs

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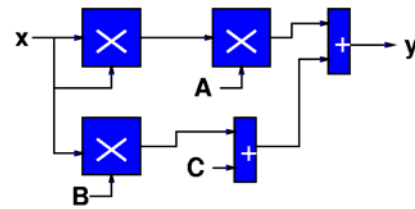
Washer/Dryer Example

- 1 Washer Takes 30 minutes
- 1 Dryer Takes 45 minutes
- How long to do one load of wash?
 - → Wash latency
- How long to do 5 loads of wash?
- Wash Throughput?

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Spatial Quadratic

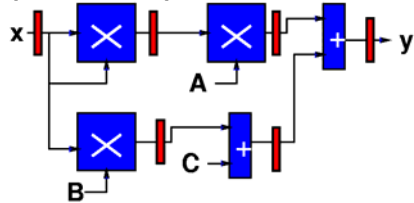


- $D(\text{Quad}) = 2 * D(\text{Mpy}) + D(\text{Add})$
- Throughput $1 / (2 * D(\text{Mpy}) + D(\text{Add}))$
- $A(\text{Quad}) = 3 * A(\text{Mpy}) + 2 * A(\text{Add})$

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Pipelined Spatial Quadratic



- $D(\text{Quad}) = 3 * D(\text{Mpy})$
- Throughput $1 / D(\text{Mpy})$
- $A(\text{Quad}) = 3 * A(\text{Mpy}) + 2 * A(\text{Add}) + 6A(\text{Reg})$

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Quadratic with Single Multiplier and Adder?

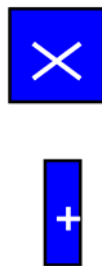
- We've seen reuse to perform the **same** operation
 - pipelining
- We can also reuse a resource in time to perform a different role.
 - Here: $x * x$, $A * (x * x)$, $B * x$
 - also: $(Bx) + c$, $(A * x * x) + (Bx + c)$

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Quadratic Datapath

- Start with one of each operation

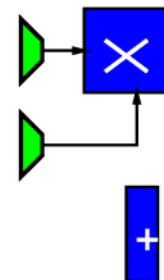


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Quadratic Datapath

- Multiplier serves multiple roles
 - $x * x$
 - $A * (x * x)$
 - $B * x$
- Will need to be able to steer data (switch interconnections)

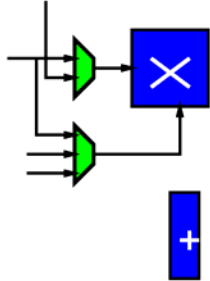


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Quadratic Datapath

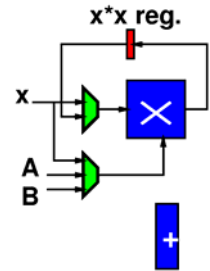
- Multiplier serves multiple roles
 - x^2
 - $A^2(x^2)$
 - B^2x
- x, x^2x
- x, A, B



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Quadratic Datapath

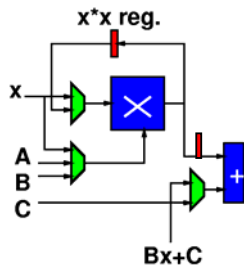
- Multiplier serves multiple roles
 - x^2
 - $A^2(x^2)$
 - B^2x
- x, x^2x
- x, A, B



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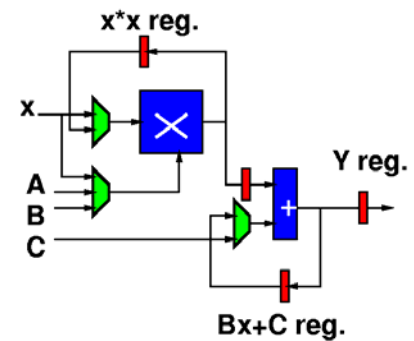
Quadratic Datapath

- Adder serves multiple roles
 - $(Bx)+c$
 - $(A^2x^2x)+(Bx+c)$
- one always mpy output
- $C, Bx+C$



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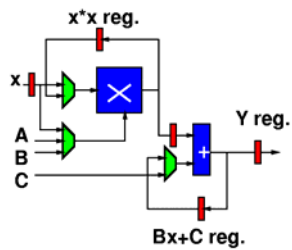
Quadratic Datapath



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Quadratic Datapath

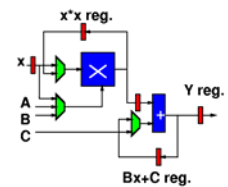
- Add input register for x



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Cycle Impact?

- Add mux delay
- Register setup/hold time, clock skew
- Limited by slowest operation



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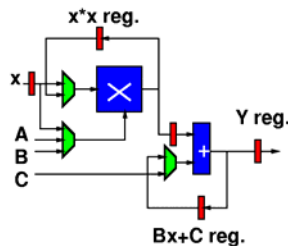
Quadratic Control

- Now, we just need to control the datapath

- What control?

- Control:

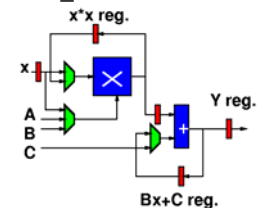
- LD X
- LD $x*x$
- MA Select
- MB Select
- AB Select
- LD $Bx+C$
- LD Y



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Quadratic Control

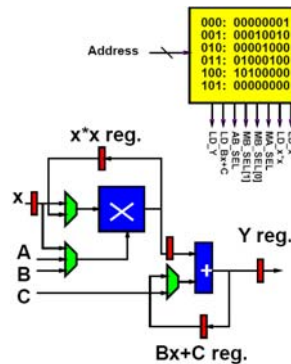
- LD_X
- MA_SEL=x, MB_SEL[1:0]=x, LD_ $x*x$
- MA_SEL=x, MB_SEL[1:0]=B
- AB_SEL=C, MA_SEL=x*x, MB_SEL=A, LD_ $Bx+C$
- AB_SEL=Bx+C, LD_Y



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Quadratic Memory Control

- LD_X
- MA_SEL=x, MB_SEL[1:0]=x, LD_ $x*x$
- MA_SEL=x, MB_SEL[1:0]=B
- AB_SEL=C, MA_SEL=x*x, MB_SEL=A, LD_ $Bx+C$
- AB_SEL=Bx+C, LD_Y

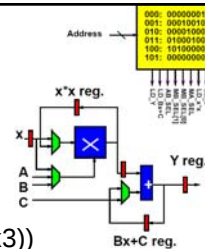


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Quadratic Datapath

- Latency/Throughput/Area?

- Latency: $5*(D(MPY)+D(\text{mux3}))$
- Throughput: $1/\text{Latency}$
- Area: $A(\text{Mpy})+A(\text{Add})+5*A(\text{Reg})+2*A(\text{Mux2})+A(\text{Mux3})+A(\text{Imem})$



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Registers→Memory

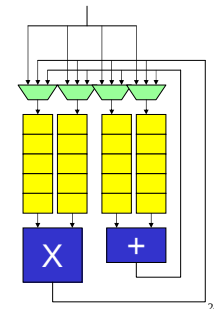
- Generally can see many registers
- If # registers $\gg$ physical operators
 - Only need to access a few at a time
- Group registers into memory banks

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Memory Bank Quadratic

- Store x
- $x*x$
- $B*x$
- $A*x^2$, $B*x+c$
- $(A*x^2)+(B*x+c)$

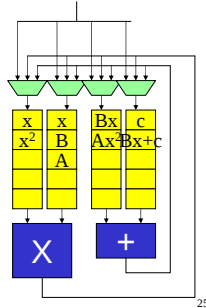


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Memory Bank Quadratic

- Store x
- $x*x$
- $B*x$
- $A*x^2$; $B*x+c$
- $(A*x^2)+(B*x+c)$

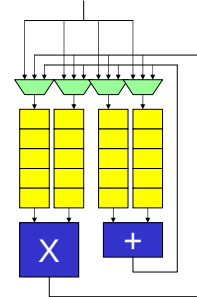


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Cycle Impact?

- Add mux delay
- Register setup/hold time, clock skew
- Memory read/write
 - Could pipeline
 - Impact?
 - Latency
 - Throughput?
- Limited by slowest operation



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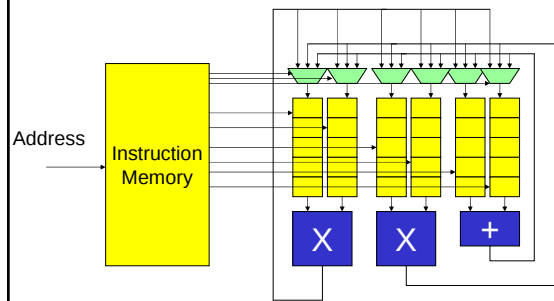
VLIW

- Very Long Instruction Word
- Set of operators
 - Parameterize number, distribution
 - Gives rise to Area-Time tradeoff
 - More operators → less time, more area
 - Fewer operators → more time, less area
- Memories for intermediate state
- Memory for "long" instructions
- Schedule compute task
- General, potentially more expensive than customized
 - Wiring, memories get expensive
 - Opportunity for further optimizations

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VLIW



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Summary

- Reuse physical operators in time
- Share operators in different roles
- Allows us to reduce area at expense of increasing time
- Area-Time tradeoff
- Pay some sharing overhead
 - Muxes, memory
- VLIW – general formulation for shared datapaths

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Admin

- Reading for Wednesday

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Big Ideas:

- Scheduled Operator Sharing