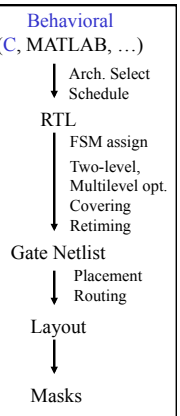
ESE535: Electronic Design Automation

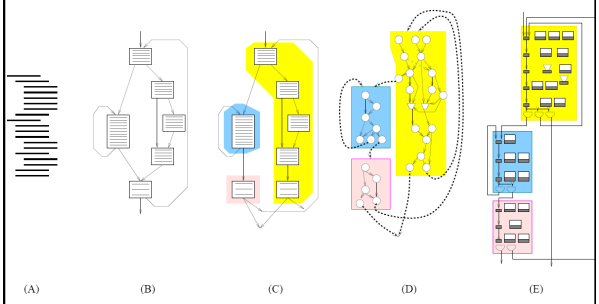
Day 15: March 13, 2013
High Level Synthesis II
Dataflow Graph Sharing

Today

Sharing
- Dataflow subgraph
  - Pattern identification
  - Pattern selection



Flow Review

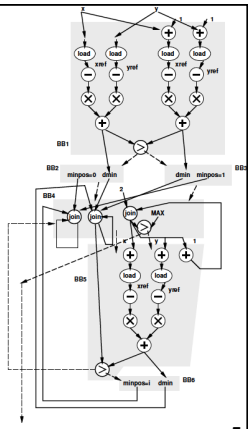


Additional Concerns?

What are we still not satisfied with?
- Parallelism in hyperblock
  - Especially if memory sequentialized
    - Disambiguate memories?
    - Allow multiple memory banks?
- Only one hyperblock active at a time
  - Share hardware between blocks?
- Data only used from one side of mux
  - Share hardware between sides?
- Most logic in hyperblock idle?
  - Couldn't we pipeline execution?

Preclass

- Common subgraphs?
- How would we like to share?
  - If trying to avoid slowdown
  - If willing to make area-time tradeoffs?



Subgraph Sharing

- Can potentially share identical subgraphs
- Can share similar subgraphs

Evaluating Subgraph Sharing

- What do we have to do to share subgraphs?
- When is it worthwhile?
  - How big does graph need to be?
  - How much overhead to share?

Example

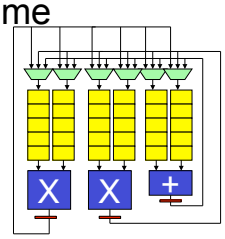
- Muxes on inputs to an adder
  - Probably bigger than just having two adders
  - 2(Amux) + Aadd > 2(Aadd)
- Muxes on input to mulitipler
  - Probably smaller than two multipliers
  - 2(Amux+Ampy) < 2(Ampy)

Extreme Case

- If ignored multiplexing overhead, what would we get?

VLIW Extreme

- Sketch
  - Each basic block requires a set of operators to achieve minimum path length
  - Union sets over all basic blocks
  - Build VLIW with that operator set
- Why unsatisfying?



Favorable Subgraphs

- Particularly beneficial when I/O into subgraph small
  - Overhead for muxing proportional to inputs

Approach

- Find candidate, reusable subgraphs
- Select a cover set of subgraphs
- Assign original graph to subgraphs
  - Assess benefits of sharing
- Patch together subgraphs with control and multiplexing

Find Subgraphs

- How might we find the set of candidate subgraphs?

Finding Subgraphs

- Keep set of subgraphs of size k
- Create subgraphs of size k+1 from subgraphs of size k
  - By adding a neighboring node
    - Maybe several such expansions for each k-subgraph
- Careful: can end up with exponential subgraphs

Optimization

- Canonicalize subgraphs so recognize when encounter same subgraph again
  - Keep set of subgraphs small

Optimization

- Compute candidate graph patterns during subgraph generation
  - Each subgraph may become a candidate
  - Keep track of subgraphs that might match with candidate subgraphs
  - As add subgraph, compare it with candidate patterns and add to list if "close" enough
  - At end of a given graph size, prune out patterns with too few potential matches

Close enough?

- **Conceptually:** not too expensive to use the candidate pattern
- **Concretely:** compute a distance metric between graph and pattern
  - Minimum cost of edits to morph one graph into another
    - E.g. relabel nodes, remove nodes
  - Want to capture potential cost of adding muxes and control

Algorithm 1 HPR Algorithm

```
1:  ℙ          → set of discovered patterns
2:  S_k        → set of size k subgraph
3:  INST(P)    → instances of a pattern P
4:  l_dist     → edit distance limit
5:  l_count    → frequency limit
6:
7:  travel all DFGs, add size 1 patterns and instances to ℙ and S_1
8:  for k ← 2,N do
9:    for all s_k ∈ S_k do
10:     adding a neighbor to expand s_k to s_{k+1}
11:     if s_k is the primary subgraph of s_{k+1} and convex then
12:       calculate CV(s_{k+1})
13:       get list of patterns P_i s.t. ||CV(P_i) − CV(s_{k+1})||_1 ≤ 4 ∗
          l_dist using LSH
14:       calculate edit distance of s_{k+1} with each P_i
15:       if d(P_i, s_{k+1}) < l_dist then
16:         add s_{k+1} to INST(P_i)
17:       else
18:         create a new pattern based on s_{k+1}, add to ℙ
19:       end if
20:       add s_{k+1} to S_{k+1}
21:     end if
22:   end for
23:   for all new pattern P_i ∈ ℙ do
24:     if |INST(P_i)| < l_count && size(P_i) ≤ (k + 1 − l_dist) then
25:       remove P_i from ℙ
26:       remove INST(P_i) from S_{k+1}
27:     end if
28:   end for
29: end for
```

[Cong & Jiang / FPGA 2008]

Cover Subgraphs

- What's our goal?

Cover Goal

- Minimize area

$$\sum_{P} A(p) + \sum_{BB} Ause(p \in P)$$

- Minimum added latency
  - Delay of BB covered by p in P

Cover Subgraph

- Given a proposed set of pattern graphs, how can we cover?

Cover Subgraph

- How many sets if we explored them all?

Greedy Cover Subgraph

- How might we cover greedily?

Greedy Cover Subgraph

- Select most beneficial pattern
- Assign it to the stuff it covers
  - Add logic to share accommodate
  - Remove those as things that need to be covered
- Repeat until all covered or no benefit

Most Beneficial Pattern

- How would we define pattern benefit?

Beneficial Pattern

- Area

$$\frac{N*(mux(io)+mux(\text{int}\,ernal))+area(P)}{N*mux(io)+area(P)}$$

- Latency $\frac{|P|}{latency(P)}$

Pattern and Graph Statistics

Size	#Subgraph	#Pattern	#Inst	#Calc
2	62	3	62	0.96
3	108	12	108	1.08
4	195	20	161	1.48
5	366	26	248	1.49
6	701	35	404	1.9
7	1357	58	579	2.6
8	2533	76	714	3.18
9	4517	86	762	3.82
10	7800	94	793	4.43
11	13112	101	668	7.04
12	21365	73	348	7.89
13	33316	32	87	5.03
14	49040	3	6	1.7

Big Ideas:

- Sharing
- Estimation
- Techniques
  - Graph Matching
  - Covering
  - Greedy

Admin

- Assignment 5a due Monday
- Reading for Monday online