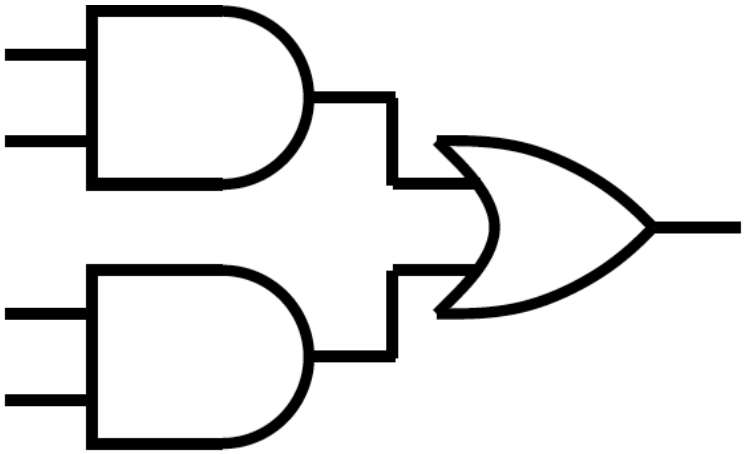
ESE535: Electronic Design Automation

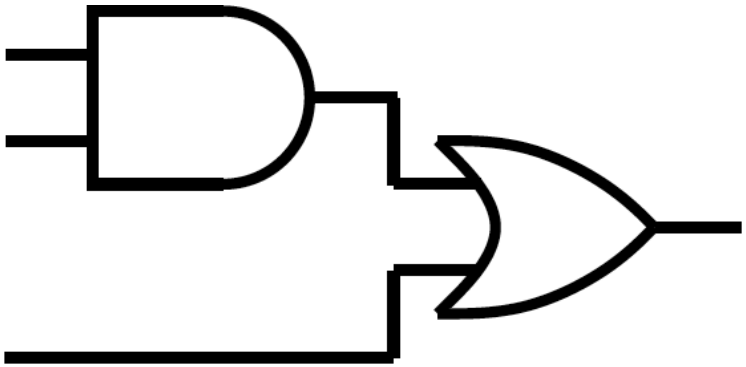
Day 24: April 22, 2015

Statistical Static Timing Analysis

Delay PDFs? (2a)



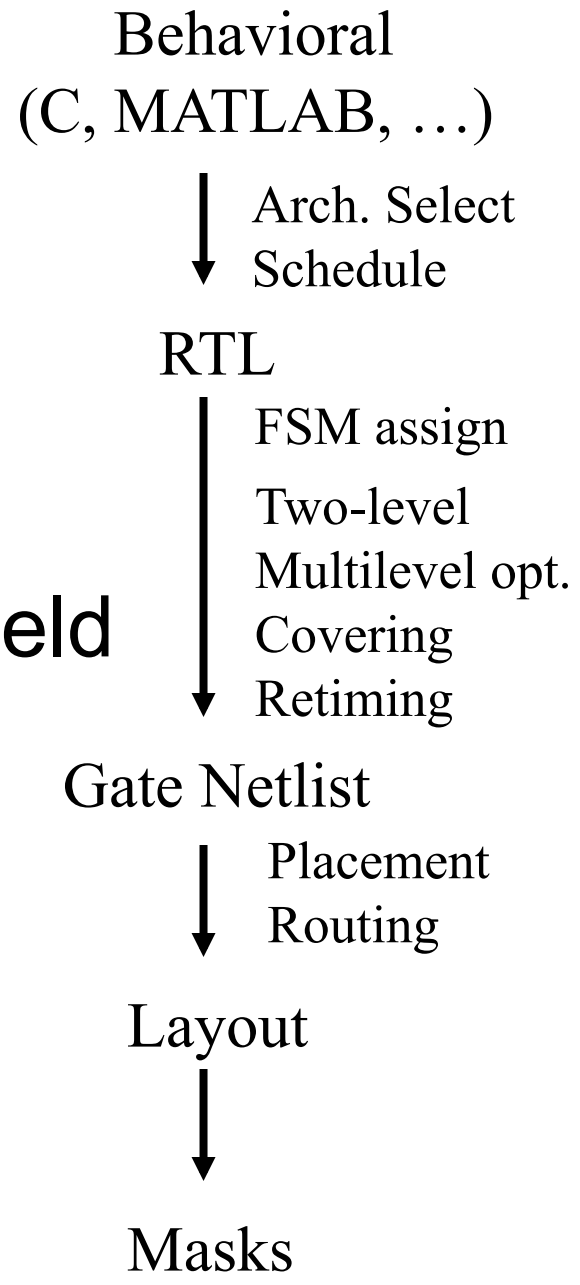
A



B

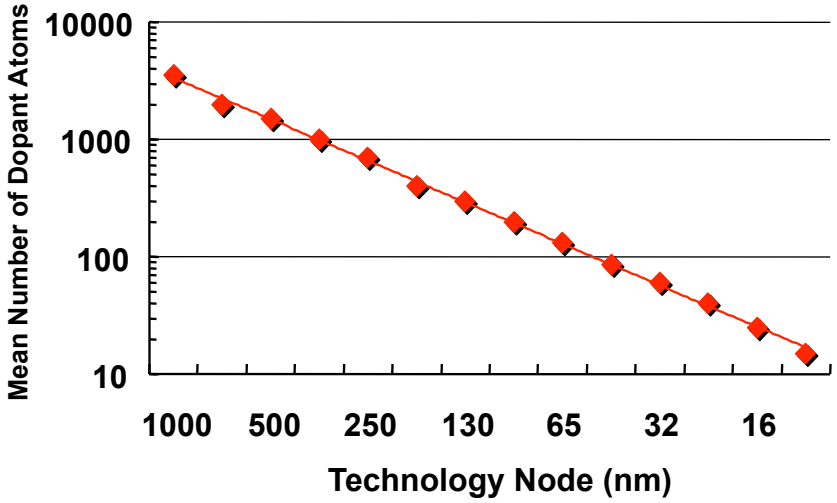
Today

- Sources of Variation
- Limits of Worst Case
- Optimization for Parametric Yield
- Statistical Analysis



Central Problem

- As our devices approach the atomic scale, we must deal with statistical effects governing the placement and behavior of individual atoms and electrons.



- Transistor critical dimensions
  - Atomic discreteness
  - Subwavelength litho
  - Etch/polish rates
  - Focus
- Number of dopants
- Dopant Placement

Oxide Thickness

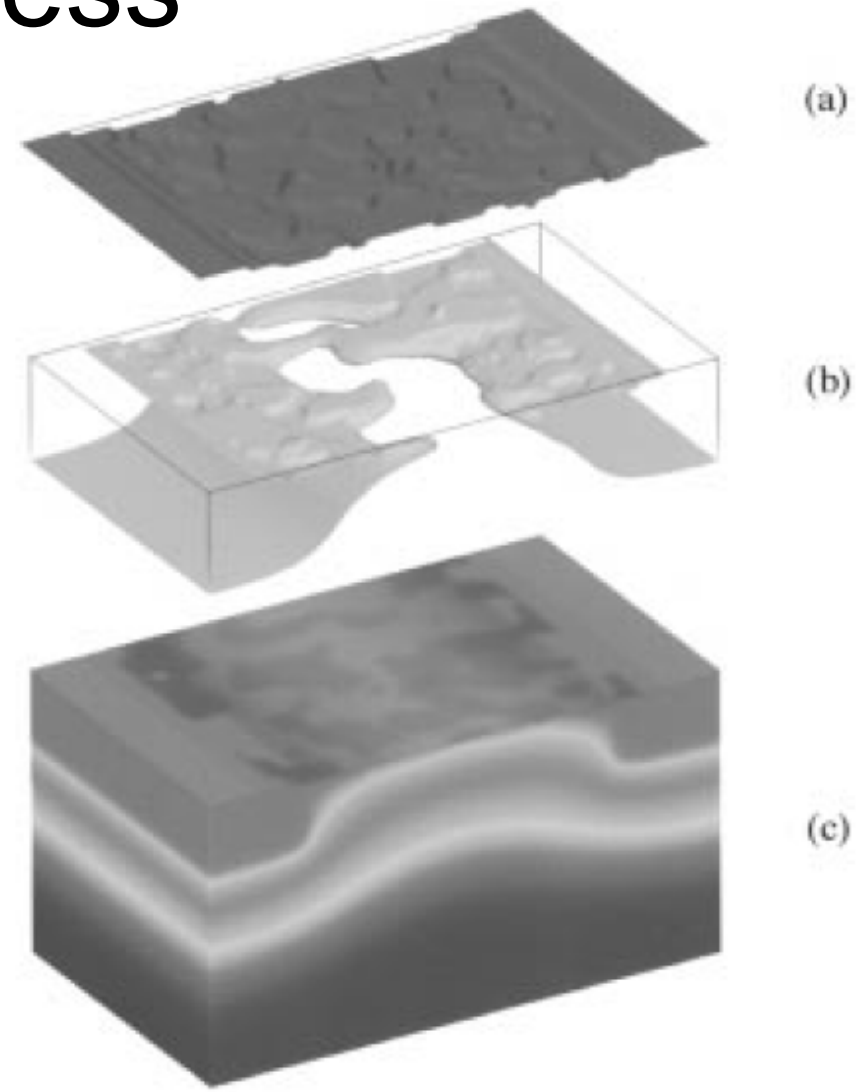
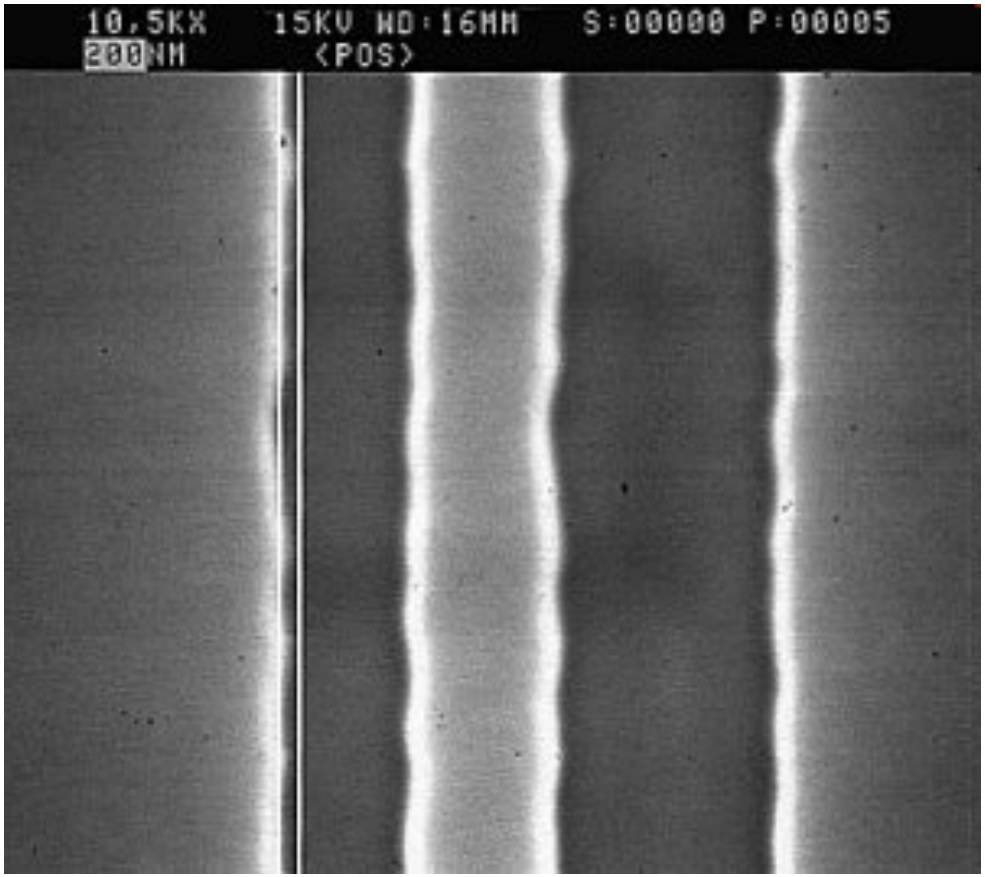


Fig. 1. (a) Typical profile of the random Si/SiO_2 interface in a 30×30 nm^2 MOSFET, followed by (b) an equiconcentration contour obtained from DG simulations, and (c) the potential distribution.

[Asenov et al. TRED 2002]

Line Edge Roughness

- 1.2μm and 2.4μm lines

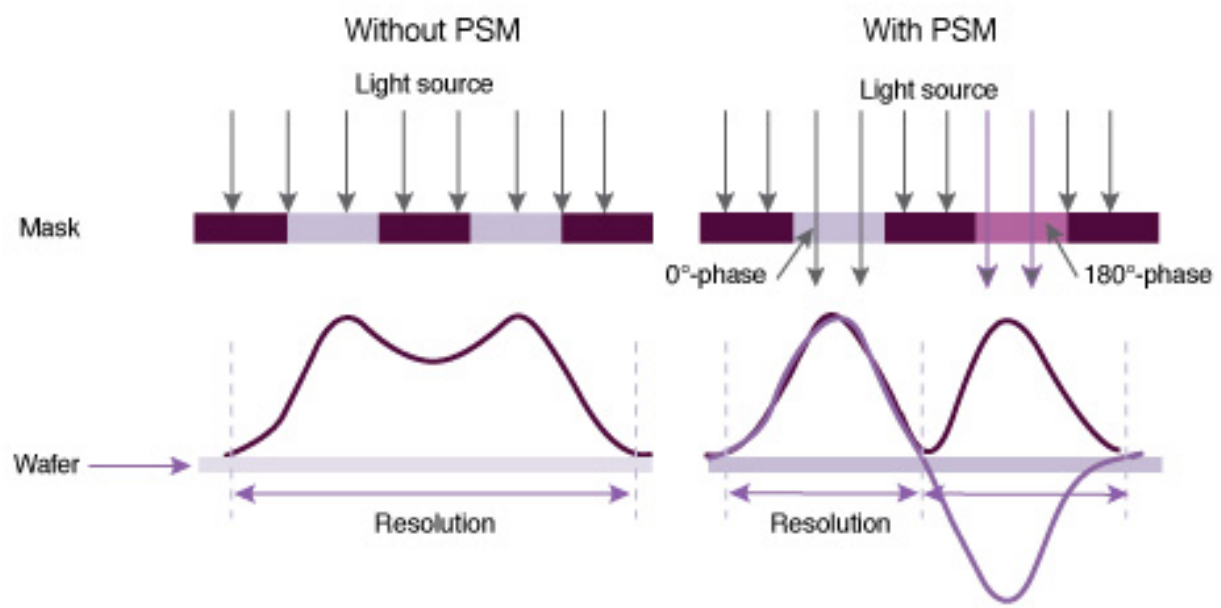


From:
http://www.microtechweb.com/2d/lw_pict.htm

Light

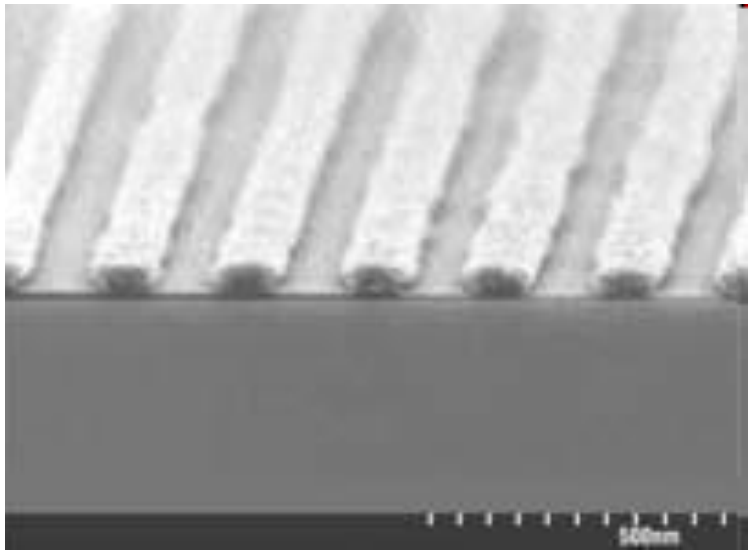
- What is wavelength of visible light?

Phase Shift Masking



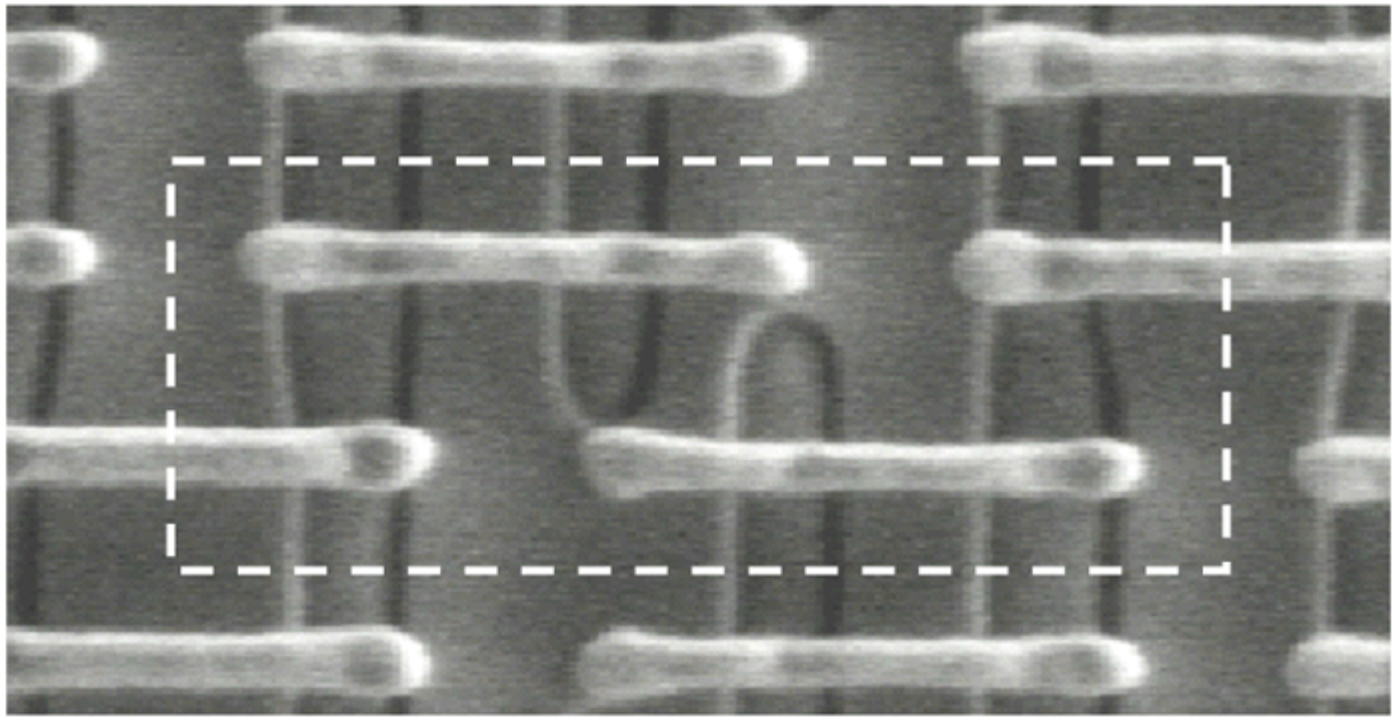
Source
http://www.synopsys.com/Tools/Manufacturing/MaskSynthesis/PSMCreate/Pages/default.aspx

Line Edges (PSM)



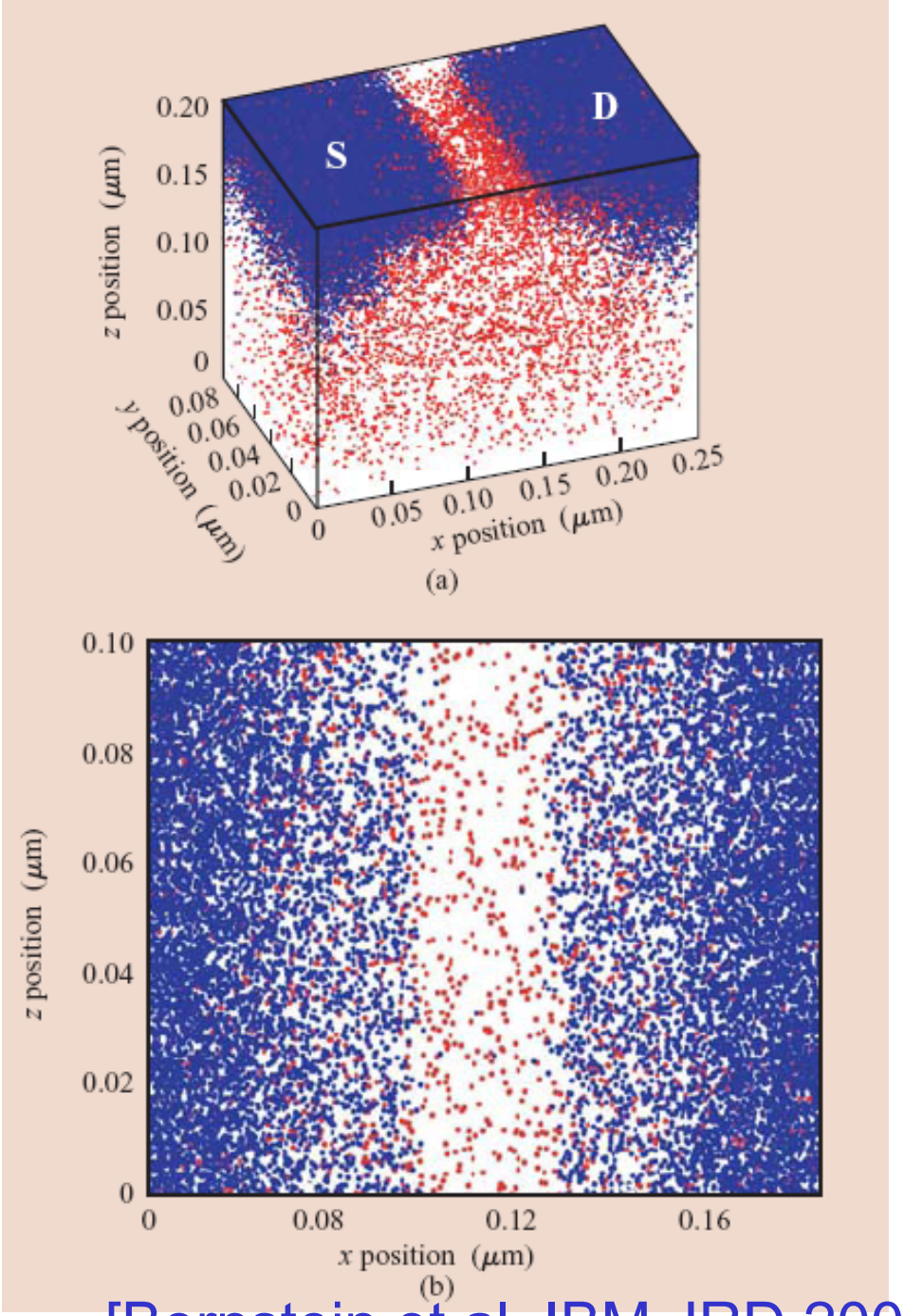
Source:
http://www.solid-state.com/display_article/122066/5/none/none/Feat/Developments-in-materials-for-157nm-photoresists

Intel 65nm SRAM (PSM)



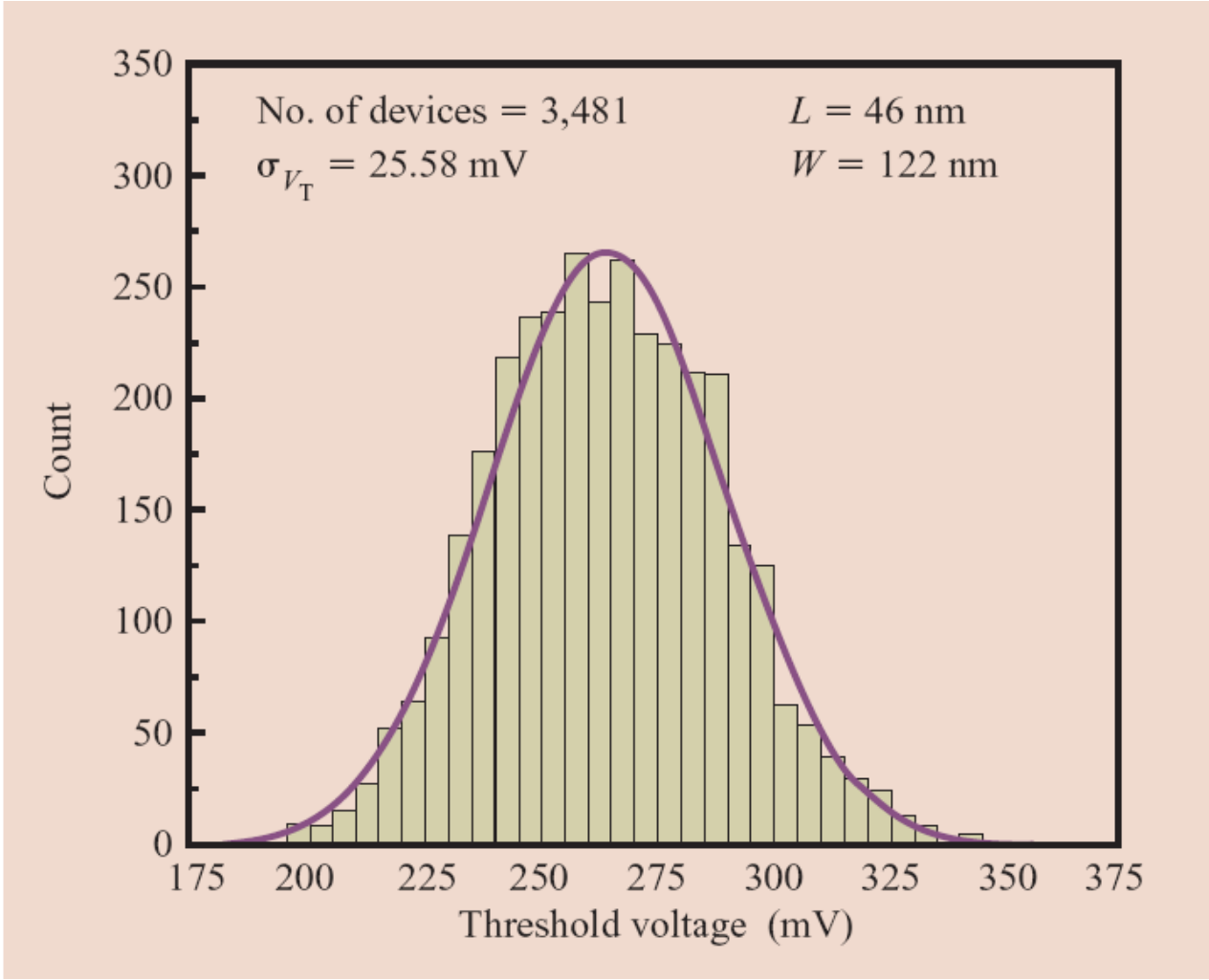
Source:
http://www.intel.com/technology/itj/2008/v12i2/5-design/figures/Figure_5_lg.gif

Statistical Dopant Placement



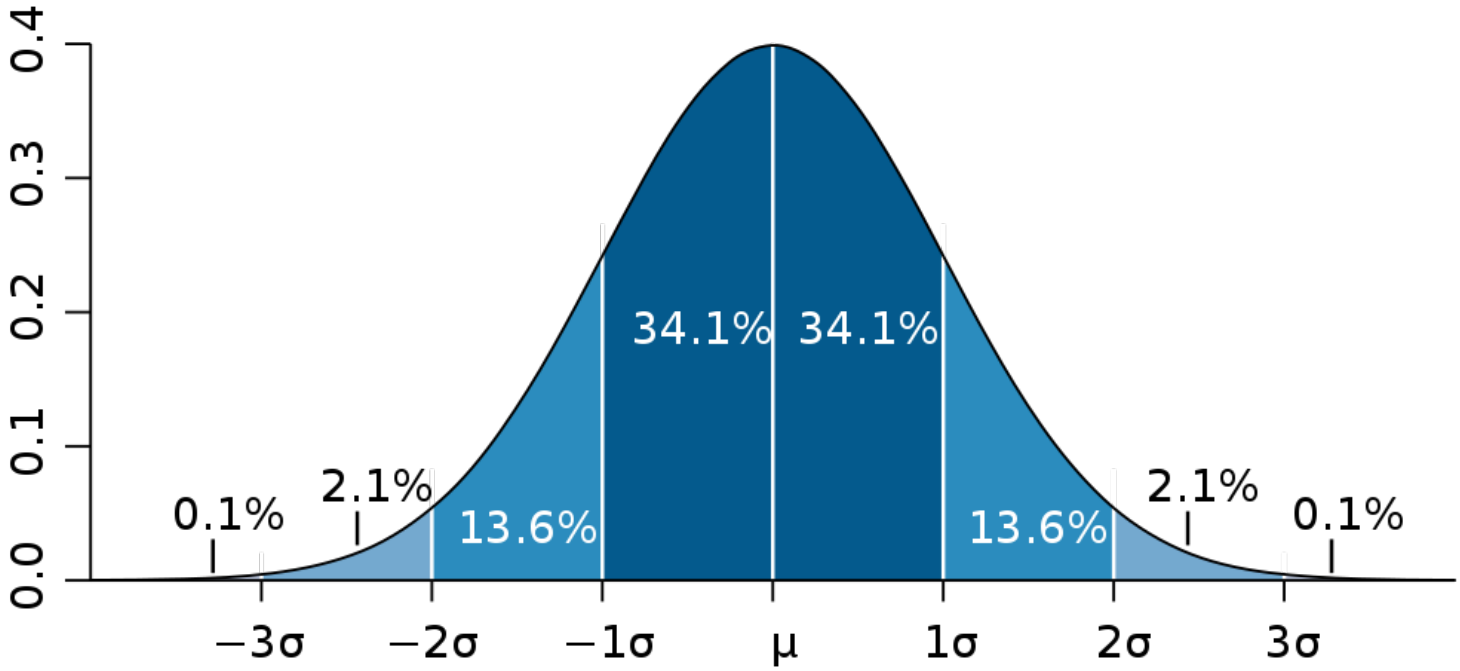
[Bernstein et al, IBM JRD 2006]

V_{th} Variability @ 65nm



[Bernstein et al, IBM JRD 2006]

Gaussian Distribution



From: http://en.wikipedia.org/wiki/File:Standard_deviation_diagram.svg

ITRS 2011 Variation (3σ)

Table DESN10 Design for Manufacturability Technology Requirements																
Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*
Normalized mask cost from public and IDM data	1.0	1.3	1.7	2.2	2.8	3.7	4.9	6.4	8.4	11.0	14.4	18.8	24.6	32.1	?	?
% V_{dd} variability: % variability seen in on-chip circuits	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%
% V_{th} variability: doping variability impact on V_{th}, (minimum size devices, memory)	40%	40%	40%	45%	45%	50%	50%	55%	55%	60%	60%	65%	65%	70%	70%	75%
% V_{th} variability: includes all sources	42%	42%	42%	47%	47%	53%	53%	58%	58%	63%	63%	68%	68%	74%	74%	79%
% V_{th} variability: typical size logic devices, all sources	20%	20%	20%	23%	23%	25%	25%	28%	28%	30%	30%	33%	33%	35%	35%	38%
% CD variability	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%	12%
% circuit performance variability circuit comprising gates and wires	42%	42%	42%	45%	45%	47%	47%	50%	50%	52%	52%	55%	55%	57%	57%	60%
% circuit total power variability circuit comprising gates and wires	51%	51%	51%	55%	55%	59%	59%	63%	63%	68%	68%	72%	72%	77%	77%	81%
% circuit leakage power variability circuit comprising gates and wires	126%	126%	126%	129%	129%	132%	132%	135%	135%	138%	138%	141%	141%	145%	145%	148%

Example: V_{th}

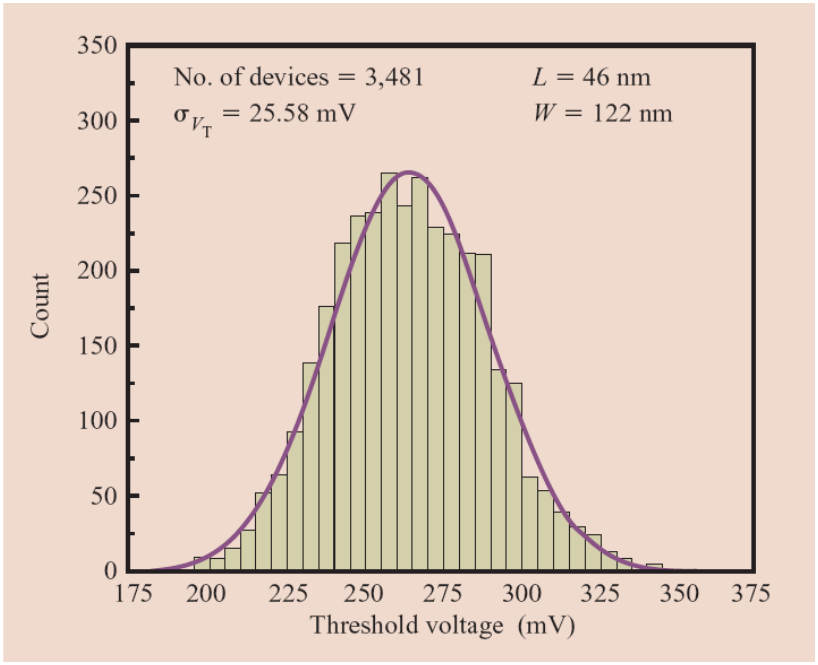
- Many physical effects impact V_{th}
  - Doping, dimensions, roughness
- Behavior highly dependent on V_{th}

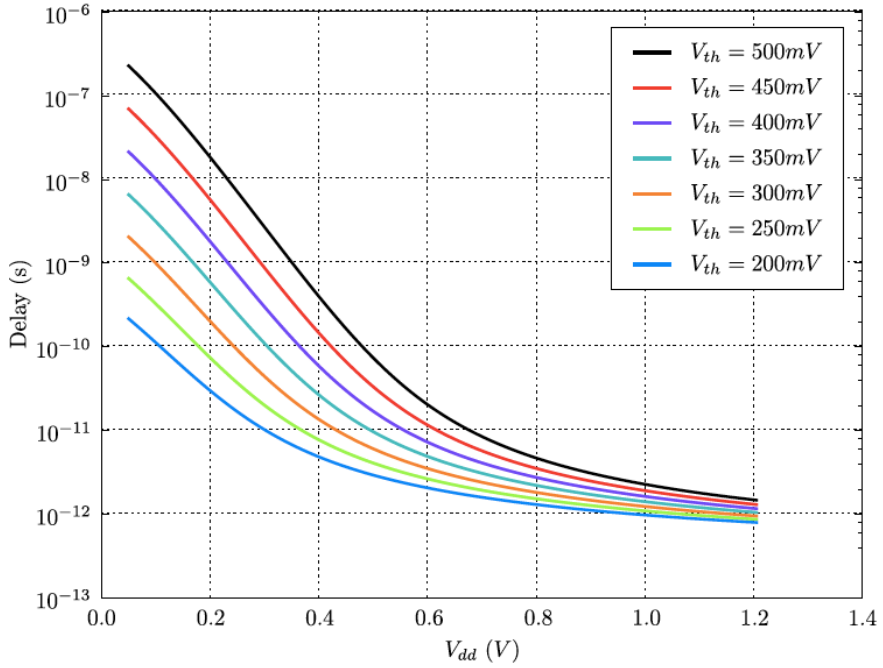
$$I_{DS} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)^2\right]$$

$$I_{DS} = I_S\left(\frac{W}{L}\right)e^{\left(\frac{V_{GS}-V_{th}}{nkT/q}\right)}\left(1 - e^{-\left(\frac{V_{DS}}{kT/q}\right)}\right)\left(1 + \lambda V_{DS}\right)$$

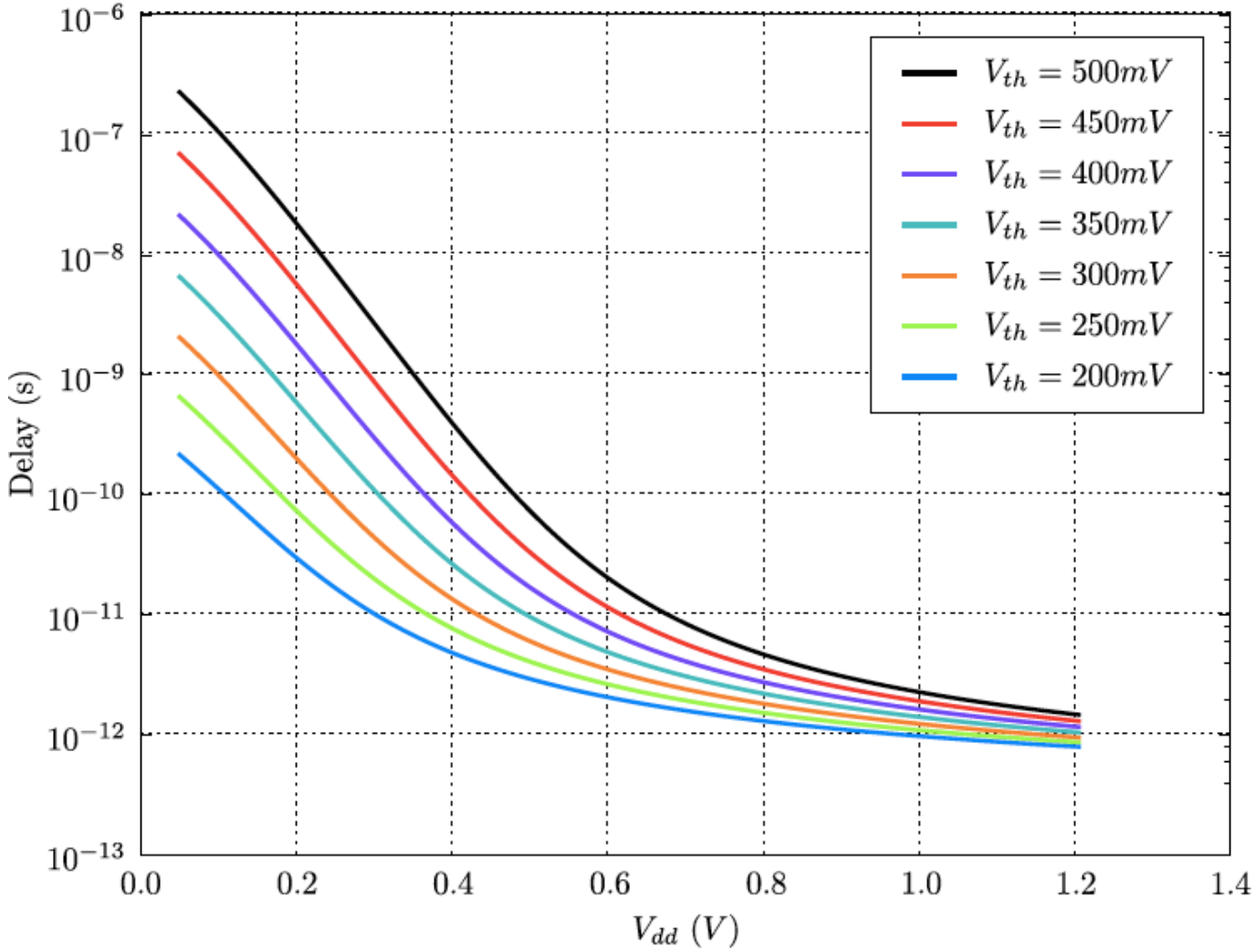
Impact Performance

- $V_{th} \rightarrow I_{ds} \rightarrow$ Delay (C_{load}/I_{ds})

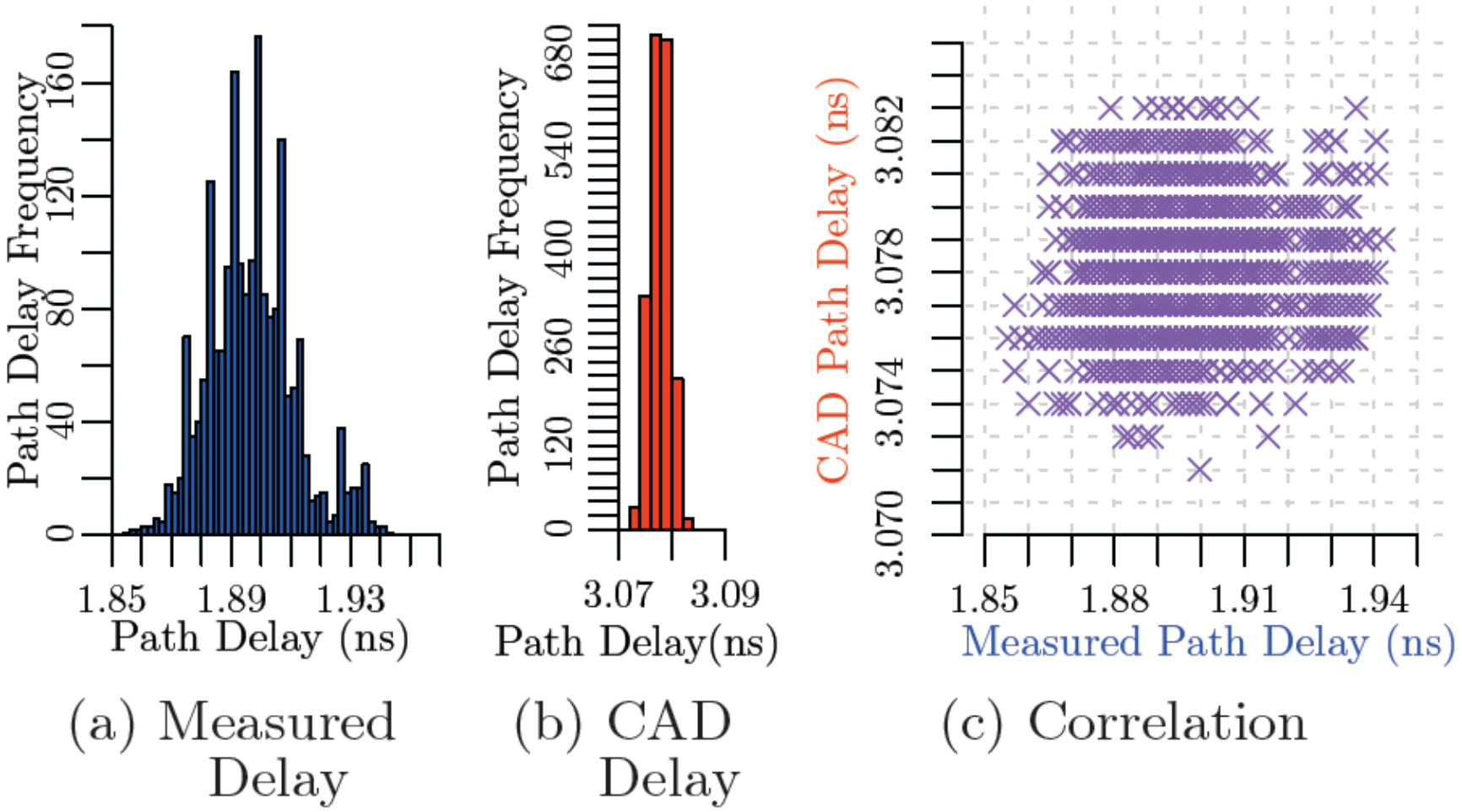




Impact of V_{th} Variation

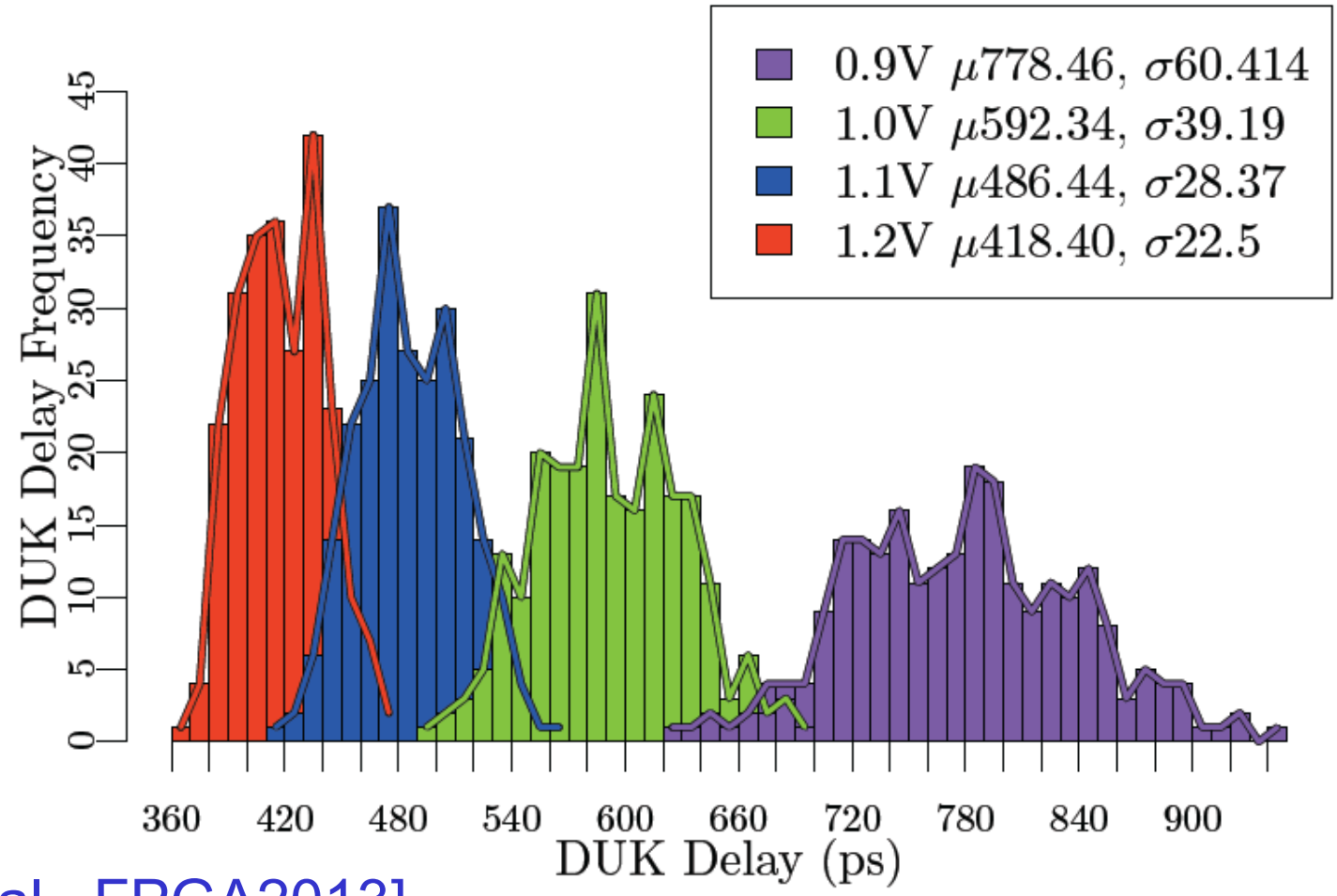


Variation in Current FPGAs



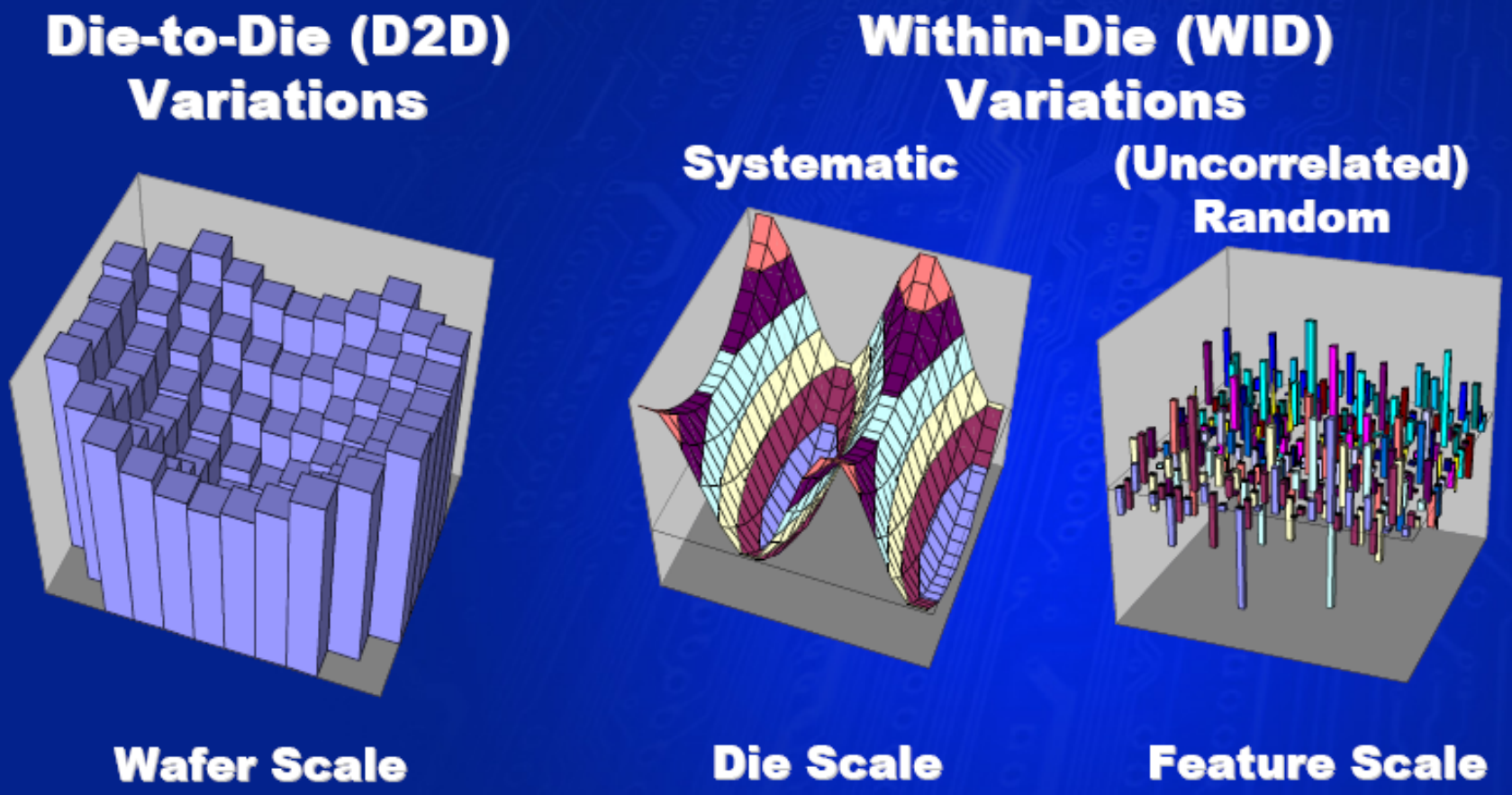
[Gojman et al., FPGA2013]

Reduce Vdd (Cyclone IV 60nm LP)



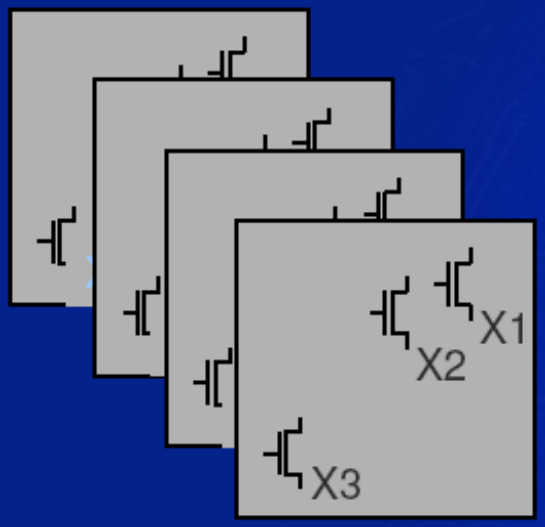
[Gojman et al., FPGA2013]

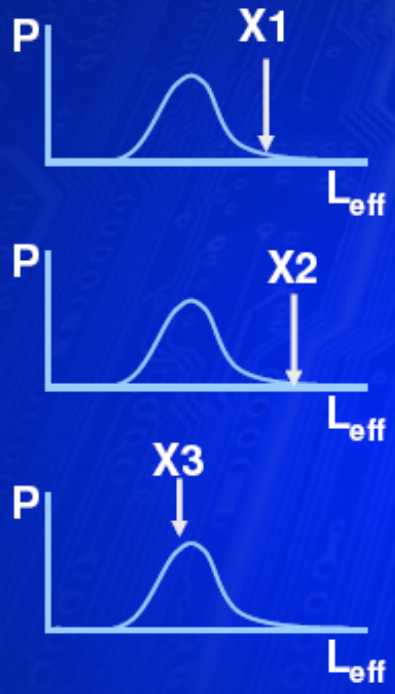
Scale of Variations

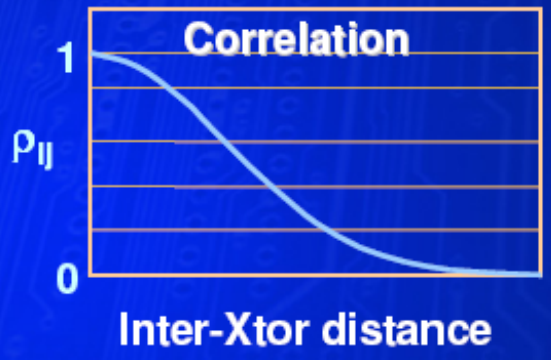


Source: Noel Menezes, Intel ISPD2007

Nature of correlated variation







- **CDs of transistors that are close track**
  - **Tracking diminishes with distance**

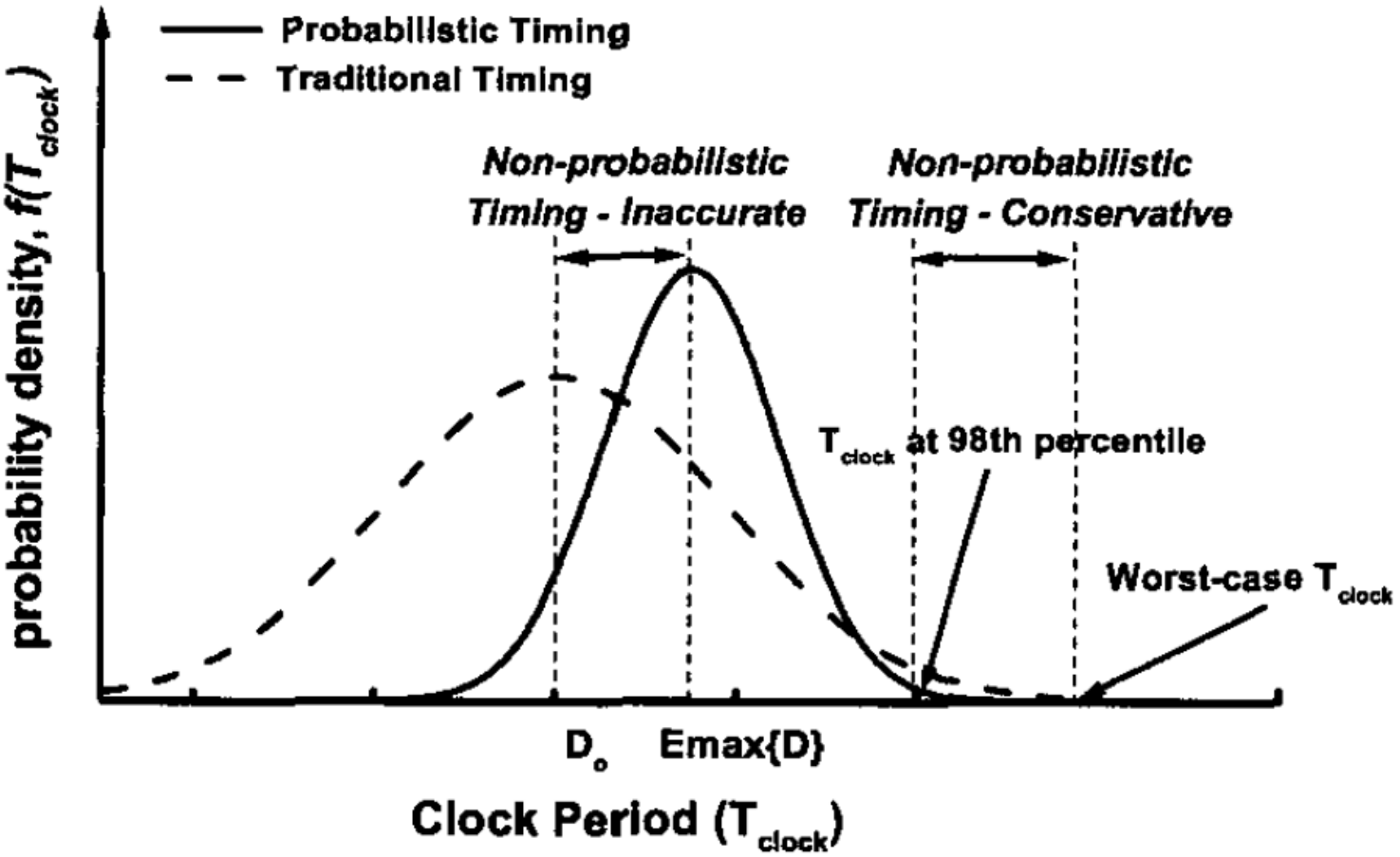
Source: Noel Menezes, Intel ISPD2007

Old Way

- Characterize gates by corner cases
  - Fast, nominal, slow
- Add up corners to estimate range

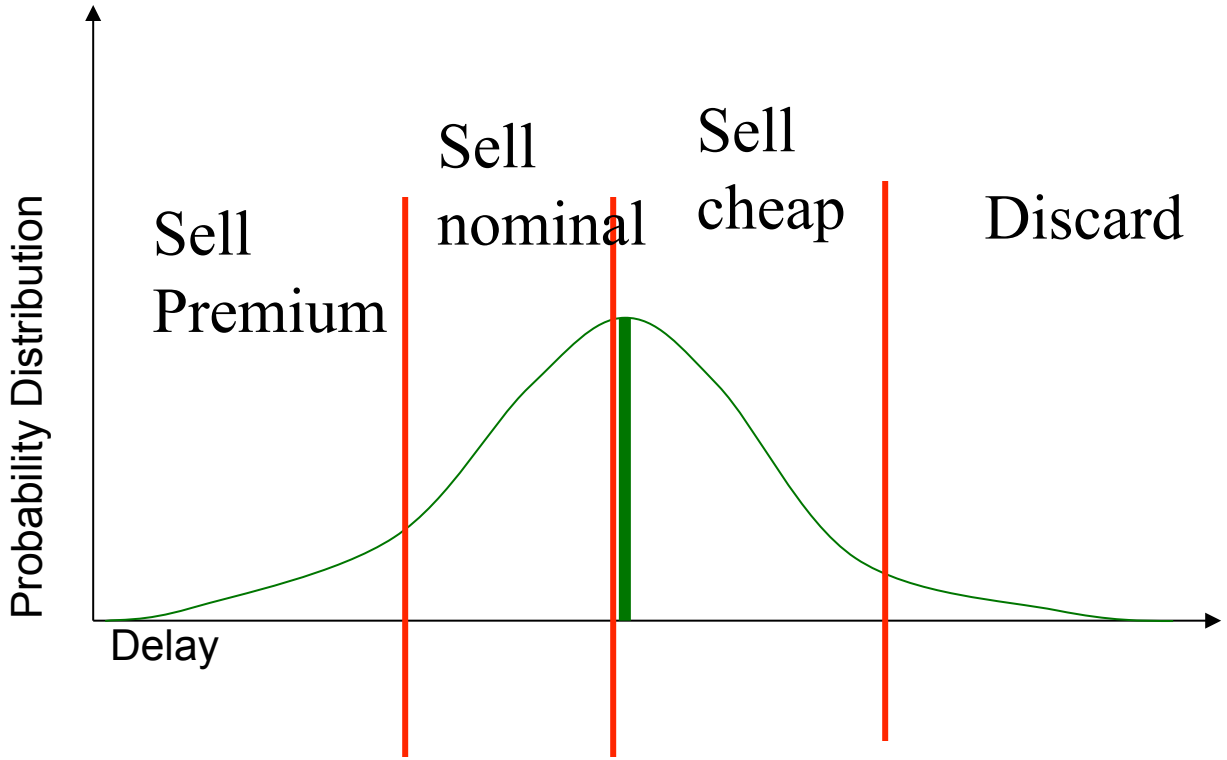
- Preclass:
  - Slow corner: 1.1
  - Nominal: 1.0
  - Fast corner: 0.9

Corners Misleading



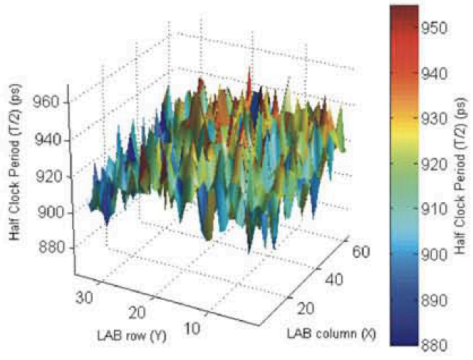
[Orshansky+Keutzer DAC 2002]

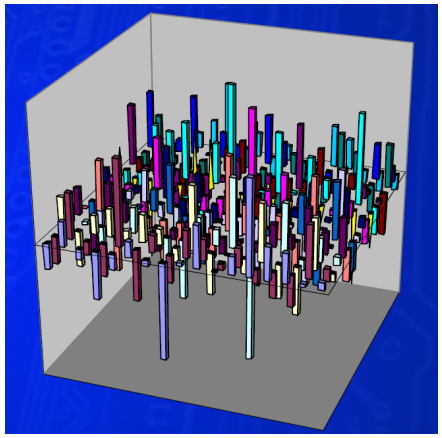
Parameteric Yield

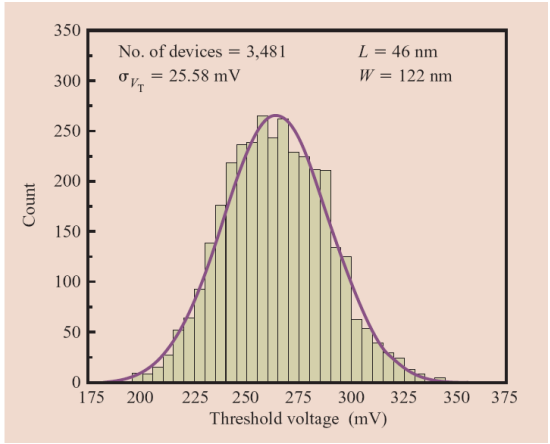


Phenomena 1: Path Averaging

- $T_{path} = t_0+t_1+t_2+t_3+\ldots t_{(d-1)}$
- T_i – iid random variables
  - Mean τ
  - Variance σ
- Tpath
  - Mean $d \times \tau$
  - Variance = $\sqrt{d} \times \sigma$







Sequential Paths

- $T_{path} = t_0+t_1+t_2+t_3+\ldots t_{(d-1)}$
- T_{path}
  - Mean $d\times\tau$
  - Variance = $\sqrt{d} \times \sigma$
- 3 sigma delay on path: $d\times\tau + 3\sqrt{d} \times \sigma$
  - Worst case per component would be: $d\times(\tau+3\ \sigma)$
  - Overestimate d vs. $\sqrt{d}$

SSTA vs. Corner Models

- STA with corners predicts 225ps
- SSTA predicts 162ps at 3σ
- SSTA reduces pessimism by 28%

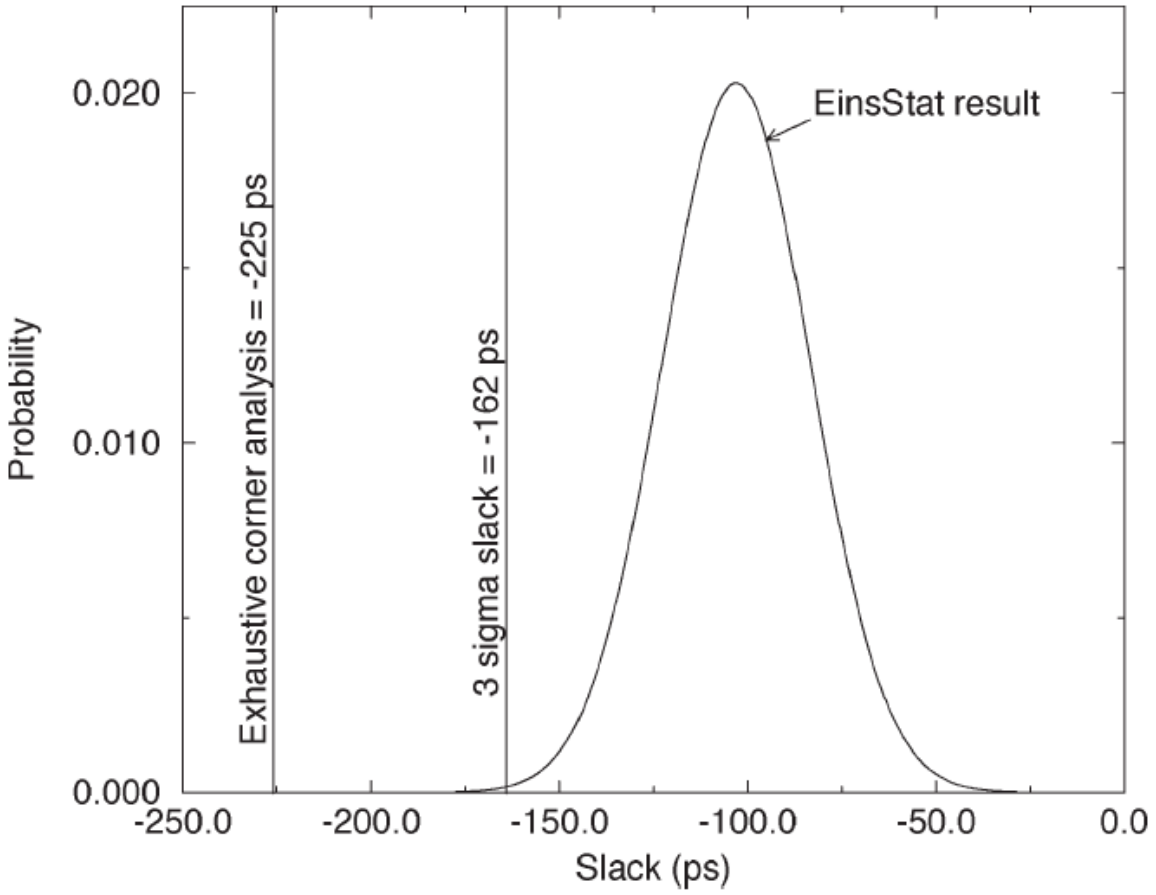


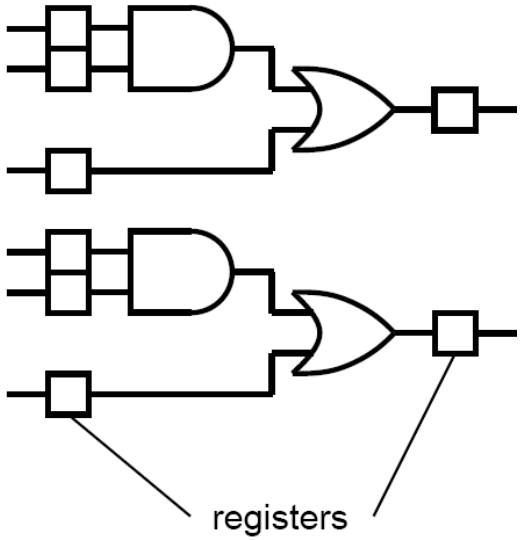
Fig. 11. EinsStat result on industrial ASIC design for early mode slacks.

[Slide composed by Nikil Mehta]

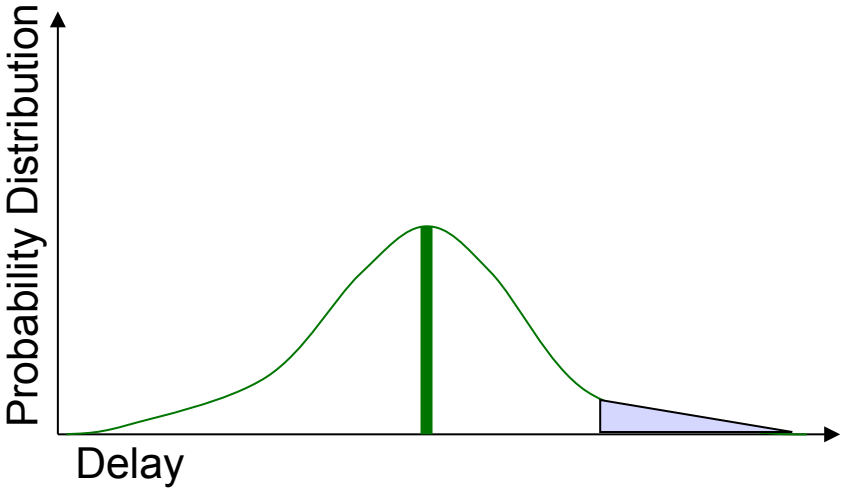
Source: IBM, TRCAD 2006

Phenomena 2: Parallel Paths

- Cycle time limited by slowest path
- $T_{cycle} = \max(T_{p0}, T_{p1}, T_{p2}, \ldots T_{p(n-1)})$
- $P(T_{cycle}<T_0) = P(T_{p0}<T_0) \times P(T_{p1}<T_0) \ldots$
- $= [P(T_p<T_0)]^n$
- $0.5 = [P(T_p<T_{50})]^n$
- $P(T_p<T_{50}) = (0.5)^{(1/n)}$

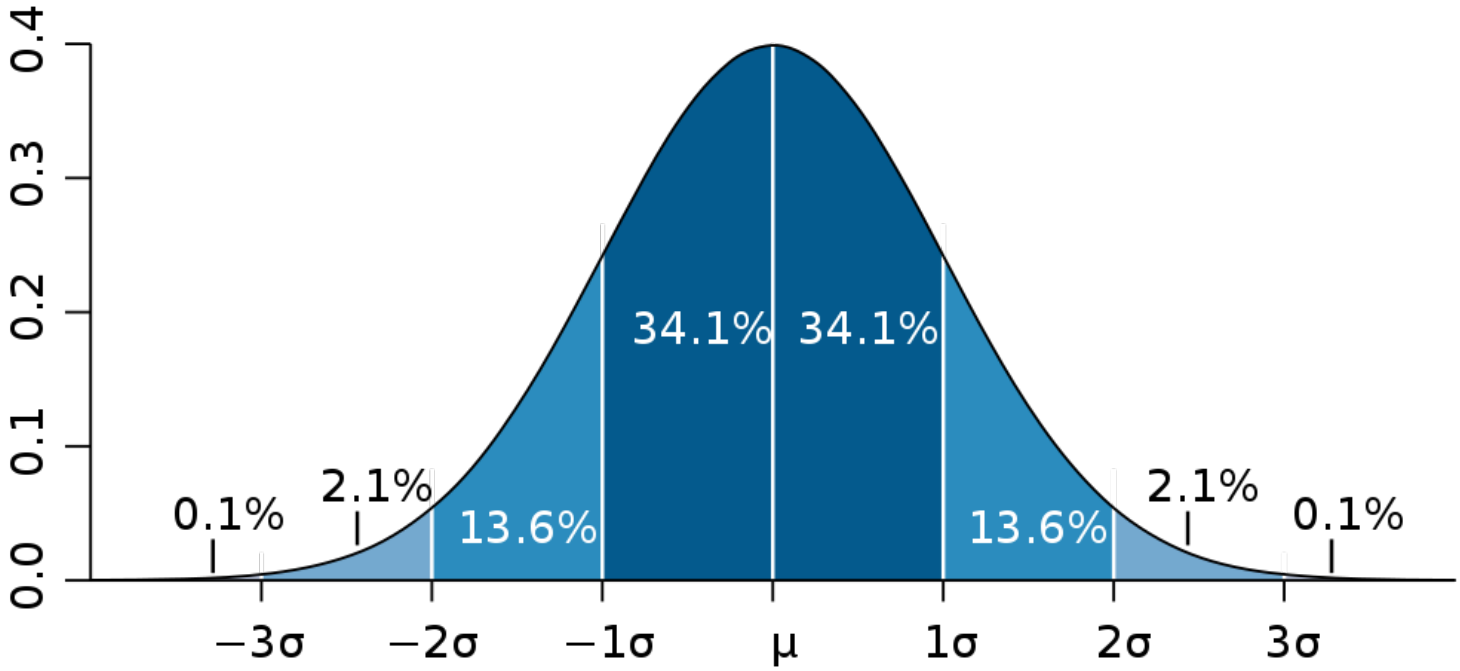


System Delay



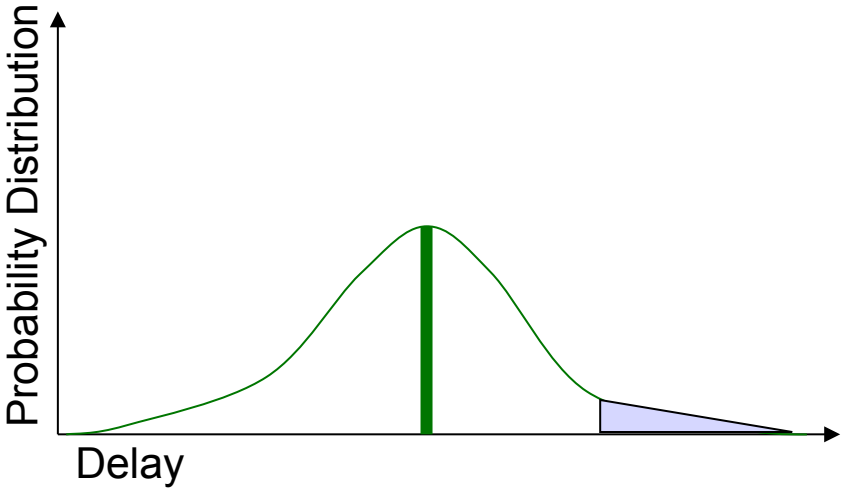
- $P(T_p<T_{50}) = (0.5)^{(1/n)}$
  - $N=10^8$ ➔ 0.999999993
    - $1-7\times10^{-9}$
  - $N=10^{10}$ ➔ 0.99999999993
    - $1-7\times10^{-11}$

Gaussian Distribution



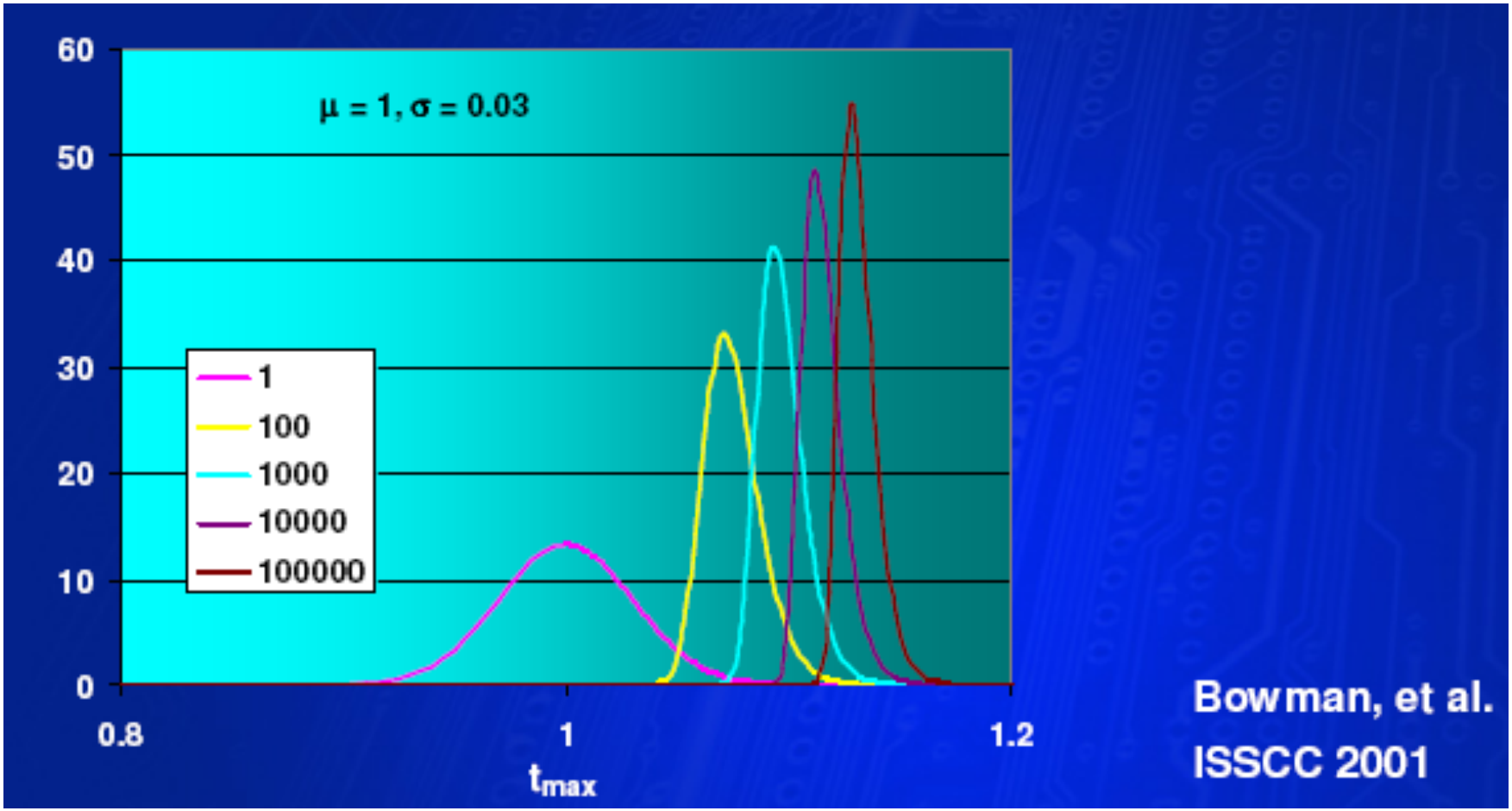
From: http://en.wikipedia.org/wiki/File:Standard_deviation_diagram.svg

System Delay

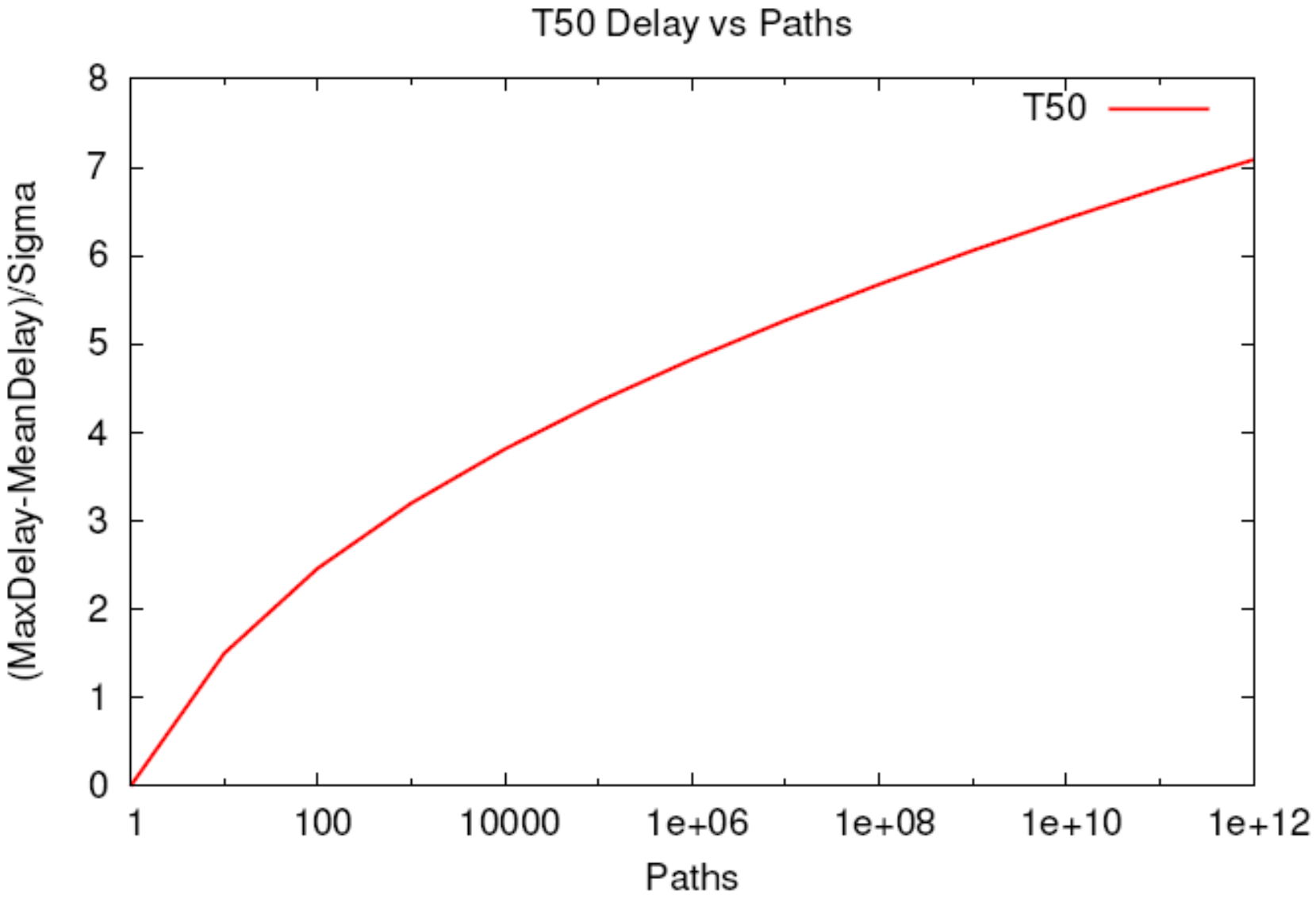


- $P(T_p<T_{50}) = (0.5)^{(1/n)}$
  - $N=10^8$ ➔ 0.999999993
    - $1-7\times10^{-9}$
  - $N=10^{10}$ ➔ 0.99999999993
    - $1-7\times10^{-11}$
- For 50% yield want
  - 6 to 7 σ
  - $T_{50}=T_{mean}+7\sigma_{path}$

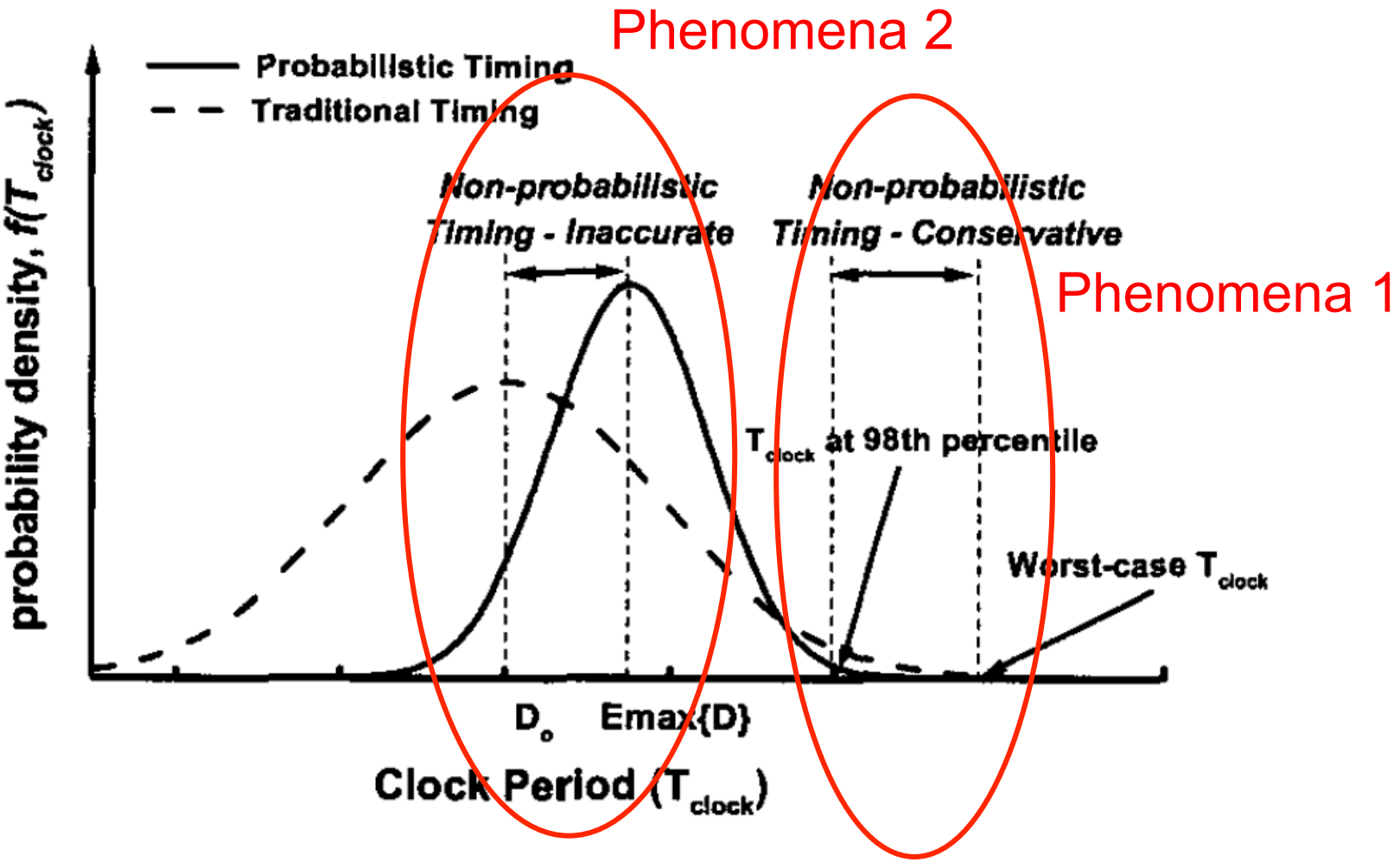
System Delay



System Delay

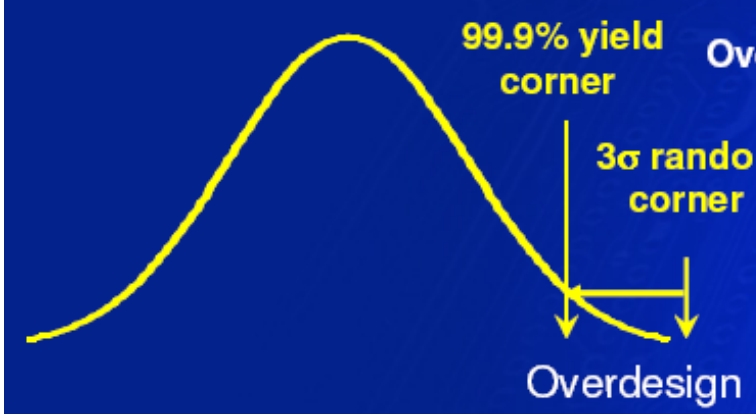


Corners Misleading

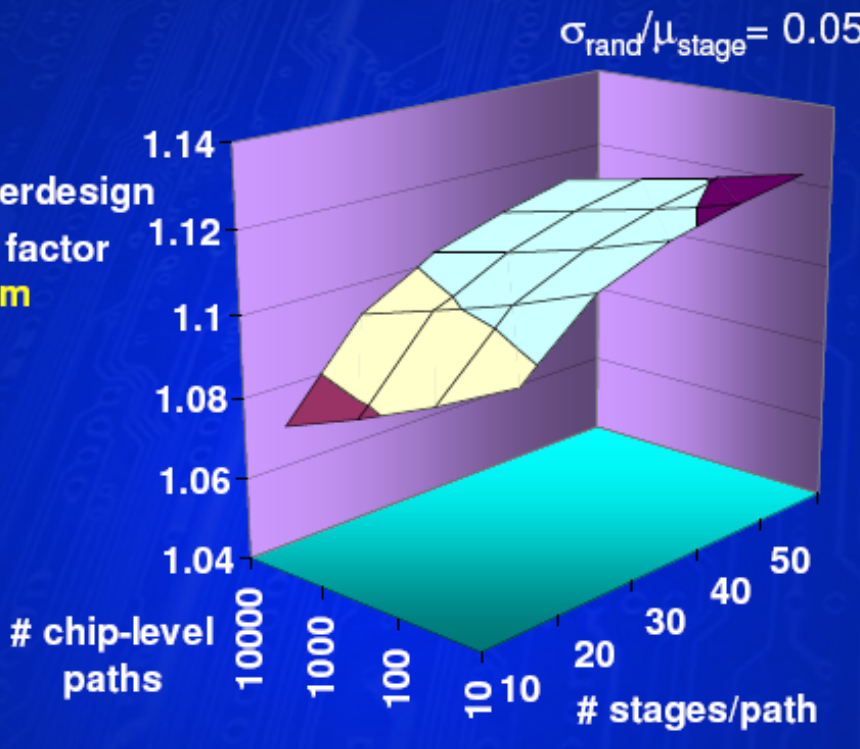


[Orshansky+Keutzer DAC 2002]

SSTA gain relative to 3σ corner analysis: Random



$$gain = \frac{1+3\sigma_{rand}}{1+\frac{\Phi^{-1}\left(Y^{1/N_p}\right)}{\sqrt{n_{cp}}}\sigma_{rand}}$$

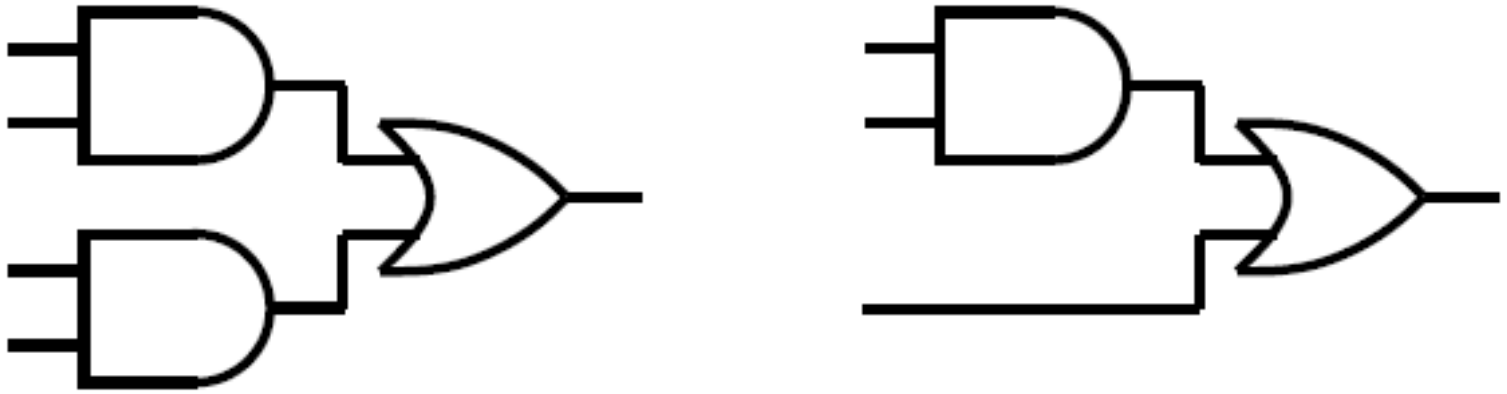


- SSTA provides a potential gain relative to a 3σ corner-based STA for purely random variation

Source: Noel Menezes, Intel ISPD2007

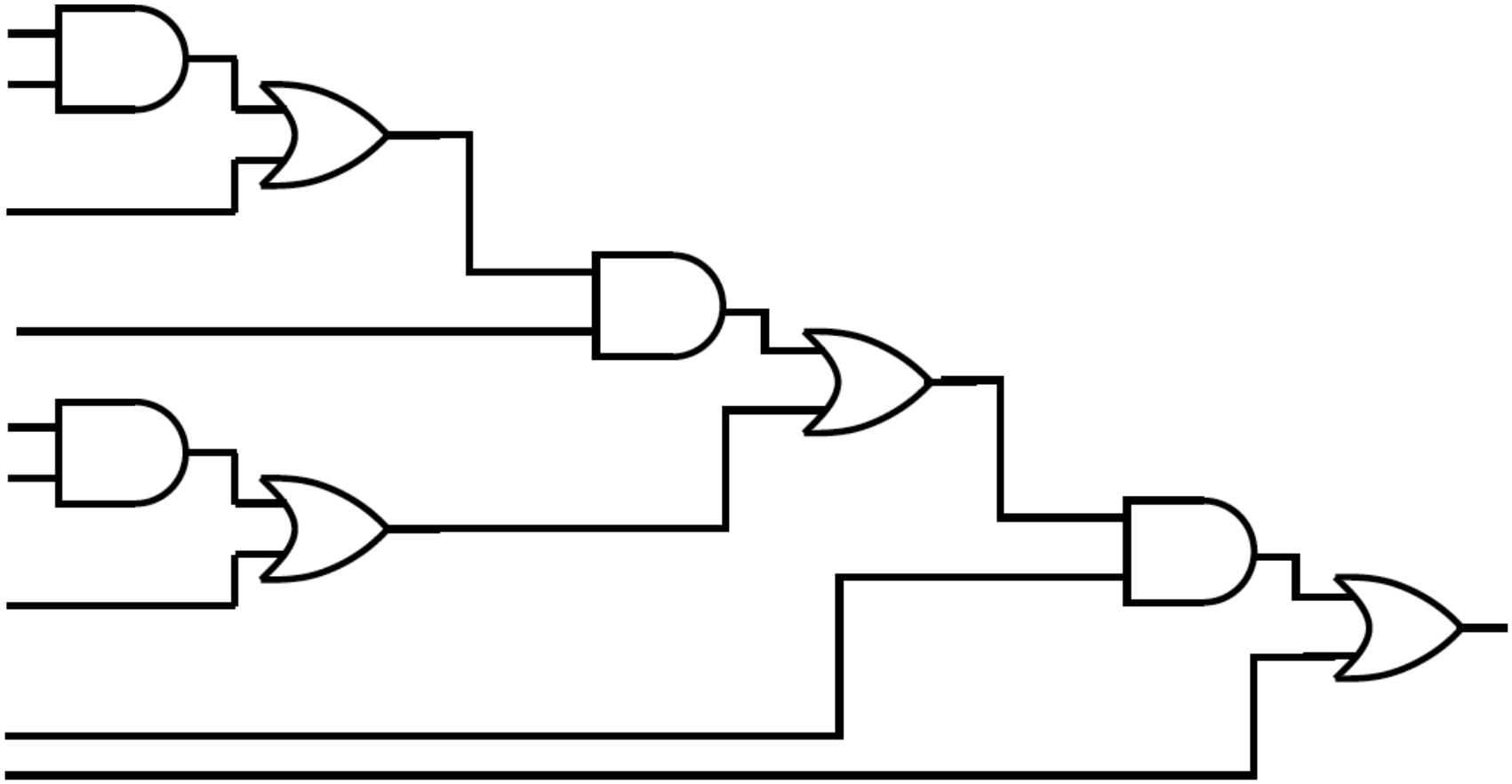
But does worst-case mislead?

- STA with worst-case says these are equivalent:



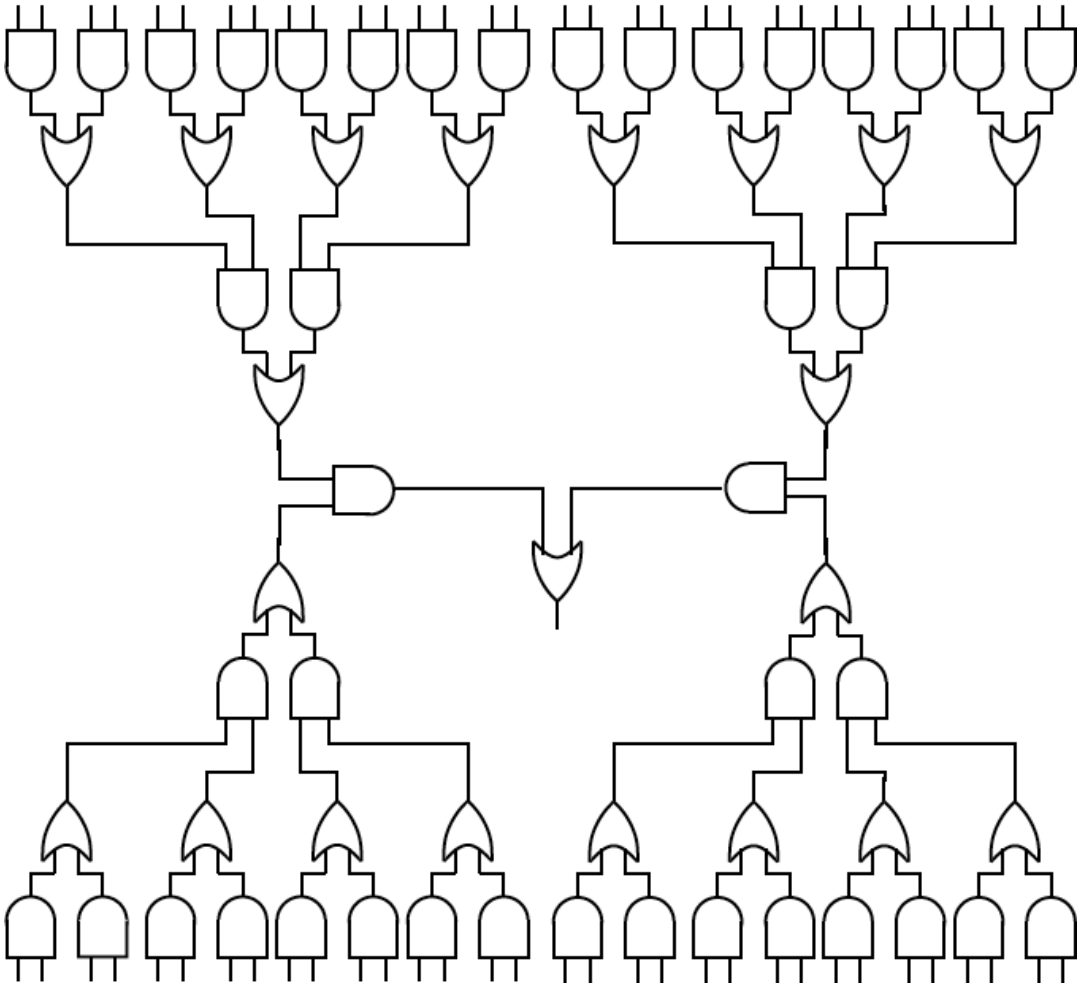
But does worst-case mislead?

- STA Worst case delay for this?



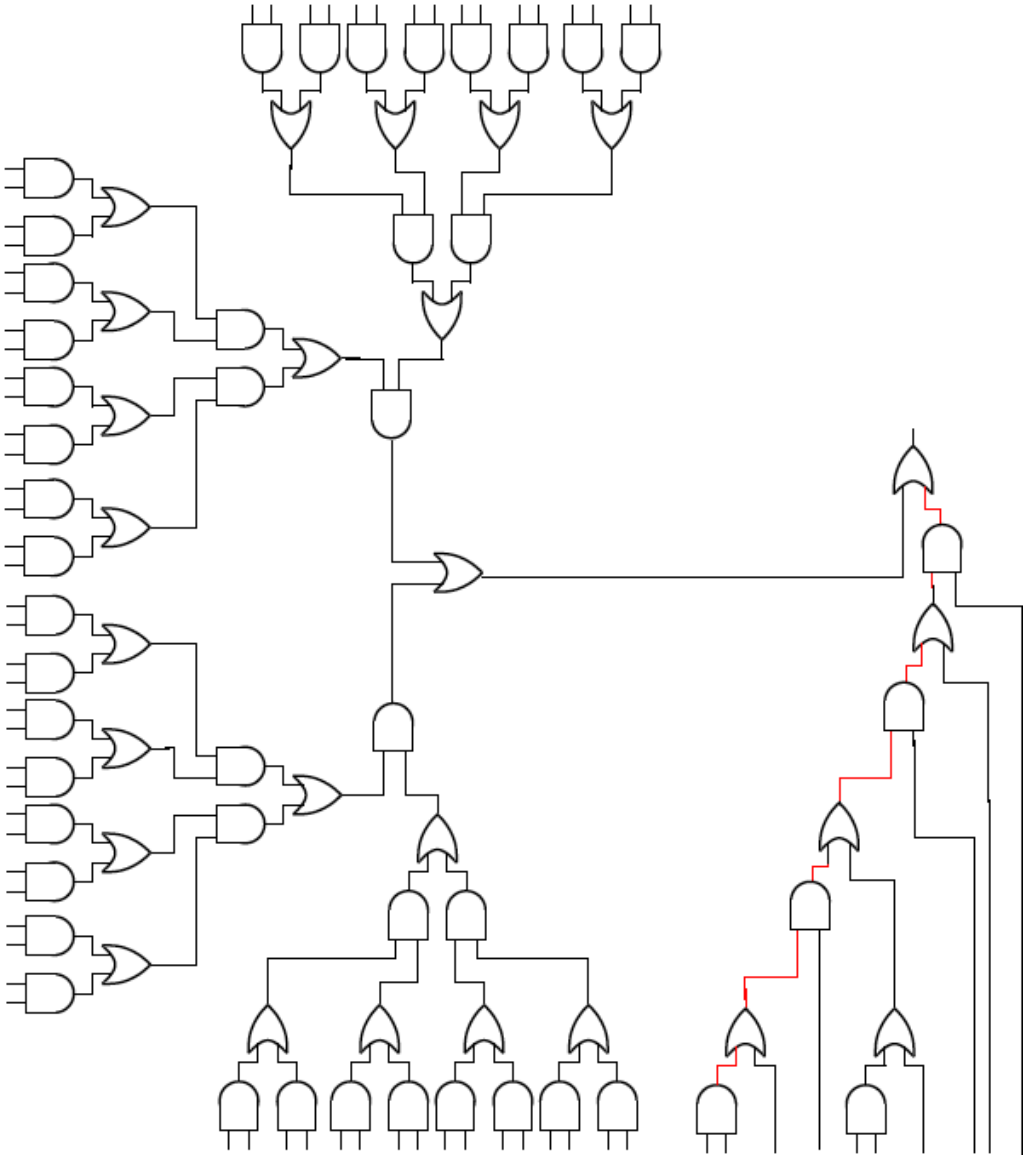
But does worst-case mislead?

- STA Worst case delay for this?



Does Worst-Case Mislead?

- Delay of off-critical path may matter
- Best case delay of critical path?
- Wost-case delay of non-critical path?



Probability of Path Being Critical

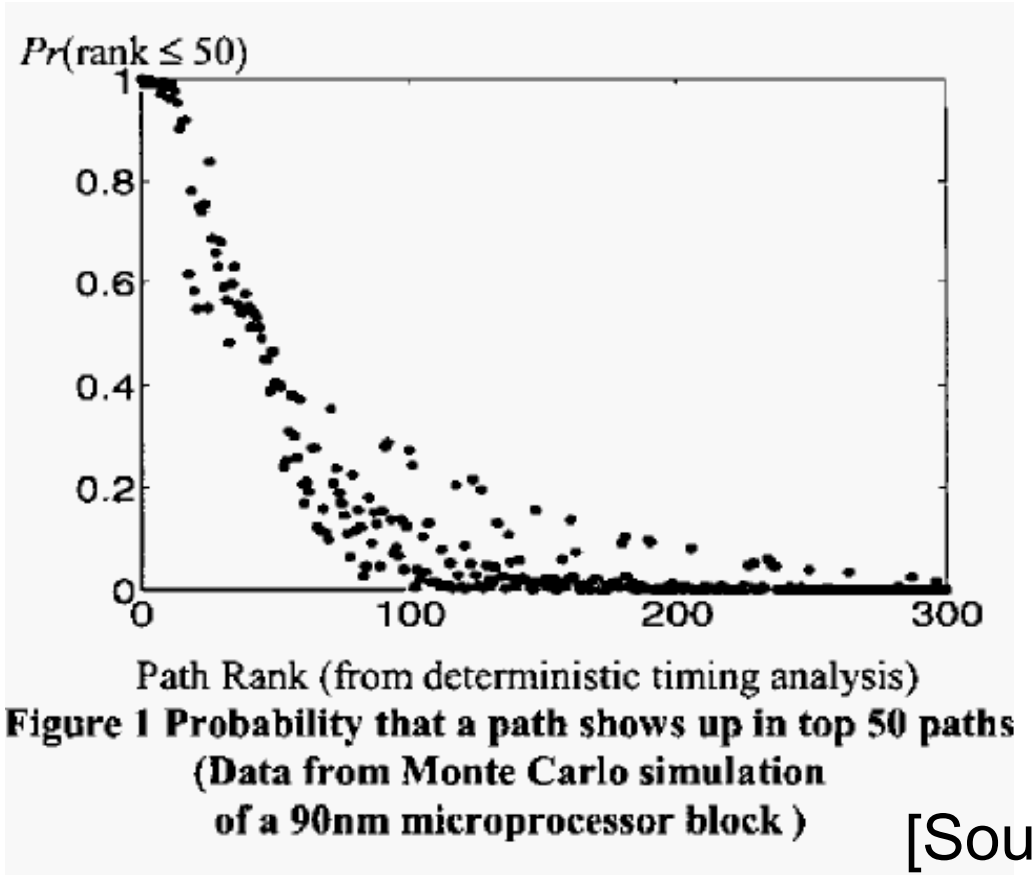


Figure 1 Probability that a path shows up in top 50 paths (Data from Monte Carlo simulation of a 90nm microprocessor block)

[Source: Intel DAC 2005]

What do we need to do?

- Ideal:
  - Compute PDF for delay at each gate
  - Compute delay of a gate as a PDF from:
    - PDF of inputs
    - PDF of gate delay

Delay Calculation

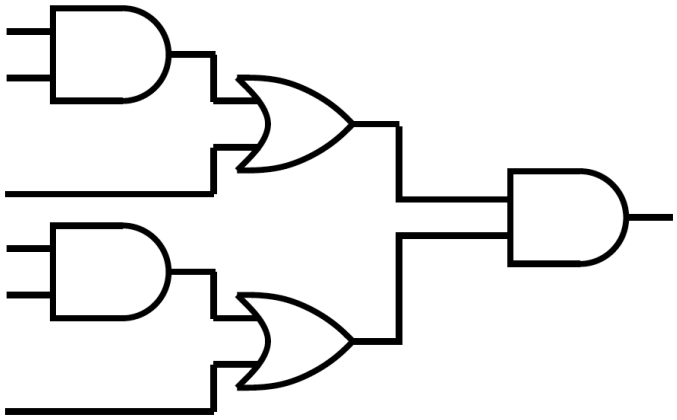
AND rules

$i_1 \rightarrow$ $i_2 \downarrow$	0	1	2
0	0 $MIN(l_1, l_2) + d$ $MIN(u_1, u_2) + d$	0 $l_2 + d$ $u_2 + d$	0 $MIN(l_1, l_2) + d$ $u_2 + d$
1	0 $l_1 + d$ $u_1 + d$	1 $MAX(l_1, l_2) + d$ $MAX(u_1, u_2) + d$	2 $l_1 + d$ $MAX(u_1, u_2) + d$
2	0 $MIN(l_1, l_2) + d$ $u_1 + d$	2 $l_2 + d$ $MAX(u_1, u_2) + d$	2 $MIN(l_1, l_2) + d$ $MAX(u_1, u_2) + d$

What do we need to do?

- Ideal:
  - compute PDF for delay at each gate
  - Compute delay of a gate as a PDF from:
    - PDF of inputs
    - PDF of gate delay
  - Need to compute for distributions
    - SUM
    - MAX (maybe MIN)

For Example

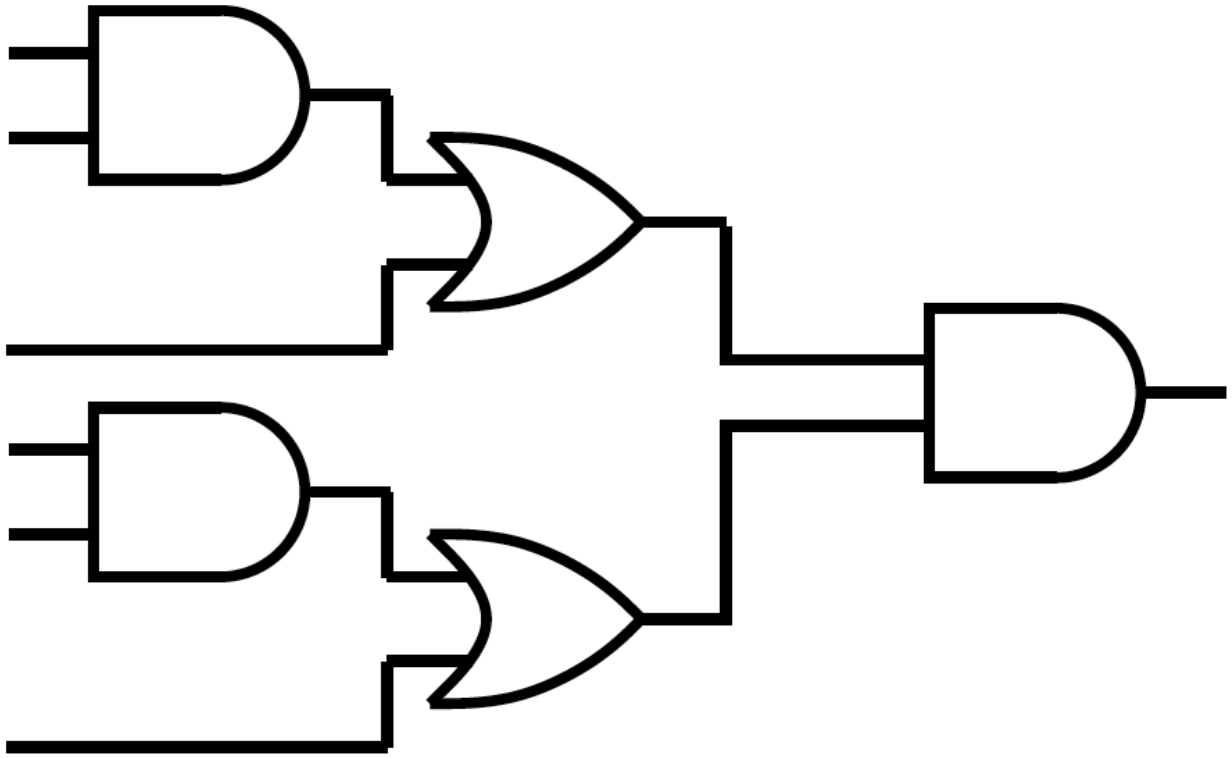


- Consider entry:
  - MAX(u_1,u_2)+d

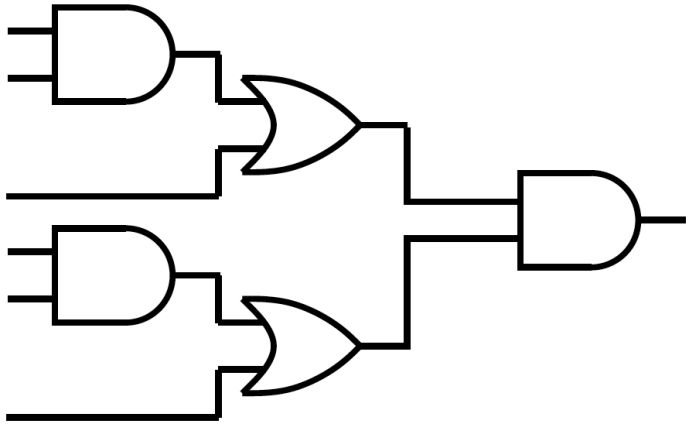
$i_1 \rightarrow$ $i_2 \downarrow$	0	1	2
0	0 $MIN(l_1, l_2) + d$ $MIN(u_1, u_2) + d$	0 $l_2 + d$ $u_2 + d$	0 $MIN(l_1, l_2) + d$ $u_2 + d$
1	0 $l_1 + d$ $u_1 + d$	1 $MAX(l_1, l_2) + d$ $MAX(u_1, u_2) + d$	2 $l_1 + d$ $MAX(u_1, u_2) + d$
2	0 $MIN(l_1, l_2) + d$ $u_1 + d$	2 $l_2 + d$ $MAX(u_1, u_2) + d$	2 $MIN(l_1, l_2) + d$ $MAX(u_1, u_2) + d$

MAX

- Compute MAX of two input distributions
  - Preclass 2(b)



SUM



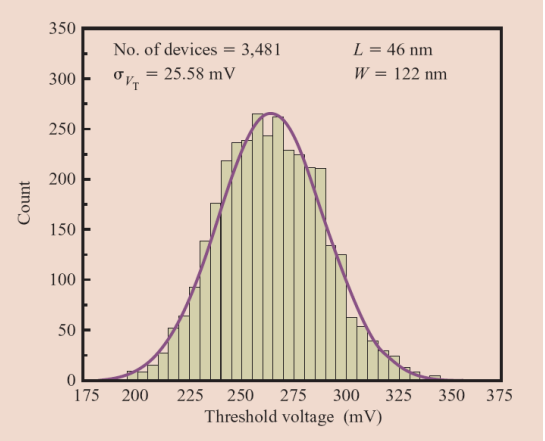
- Add that distribution to gate distribution.

Continuous

- Can roughly carry through PDF calculations with Guassian distributions rather than discrete PDFs

Dealing with PDFs

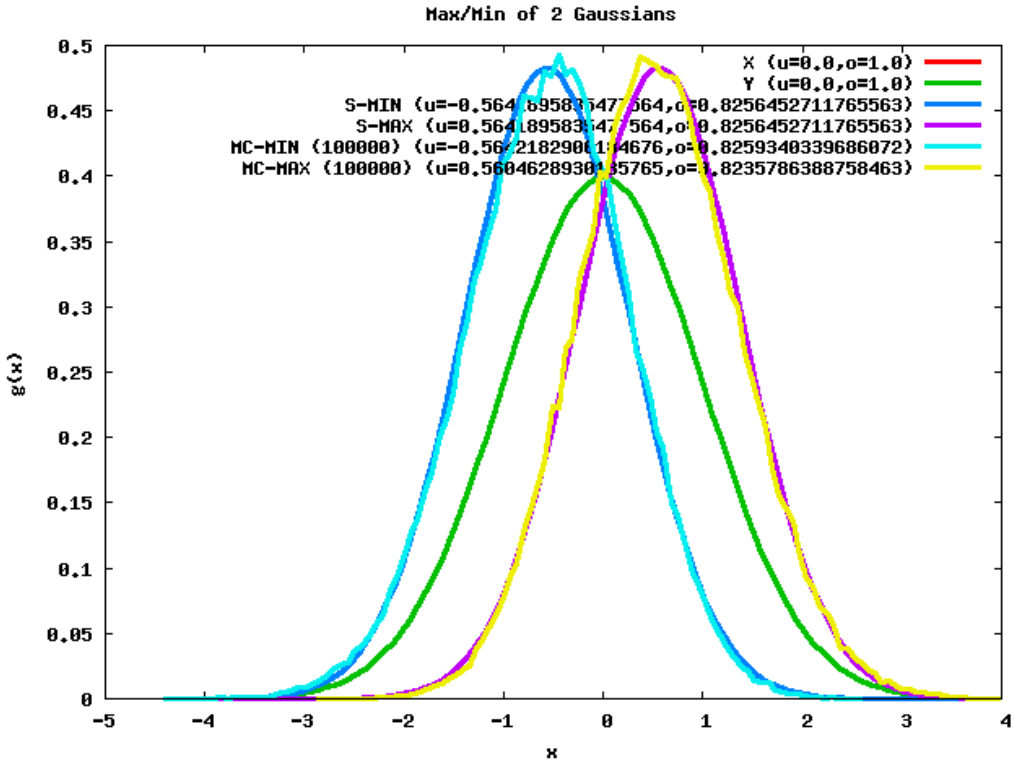
- Simple model assume all PDFs are Gaussian
  - Model with mean, σ
  - Imperfect
    - Not all phenomena are Gaussian
    - Sum of Gaussians is Gaussian
    - Max of Gaussians is **not** a Gaussian



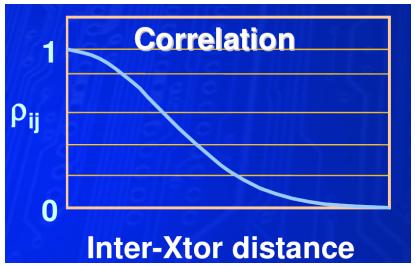
MAX of Two Identical Gaussians

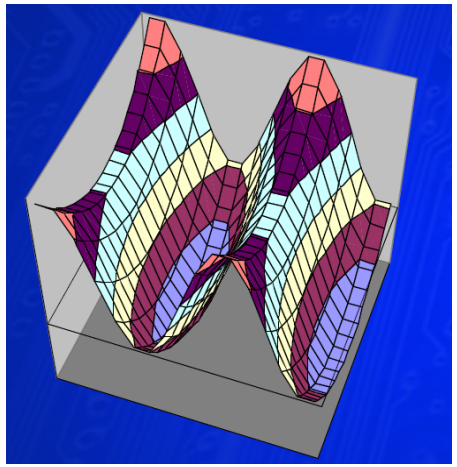
- Max of Gaussians is not a Gaussian
- Can try to approximate as Guassian
- Given two identical Gaussians A and B with μ and σ
- Plug into equations
- $E[MAX(A,B)] = \mu + \sigma/(\pi)^{1/2}$
- $VAR[MAX(A,B)] = \sigma^2 - \sigma/\pi$

[Source: Nikil Mehta]

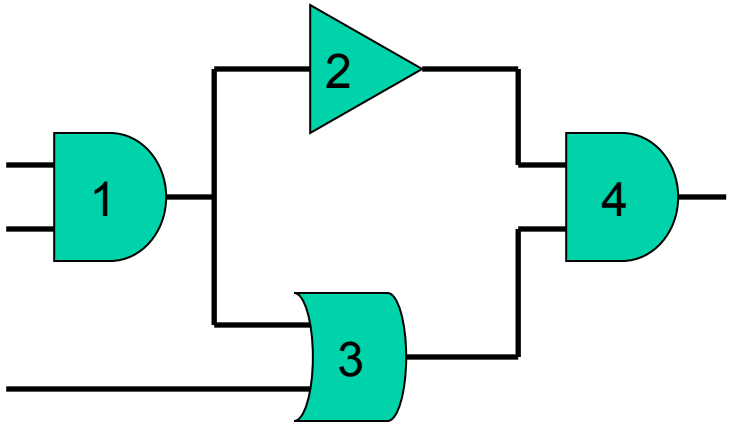


More Technicalities



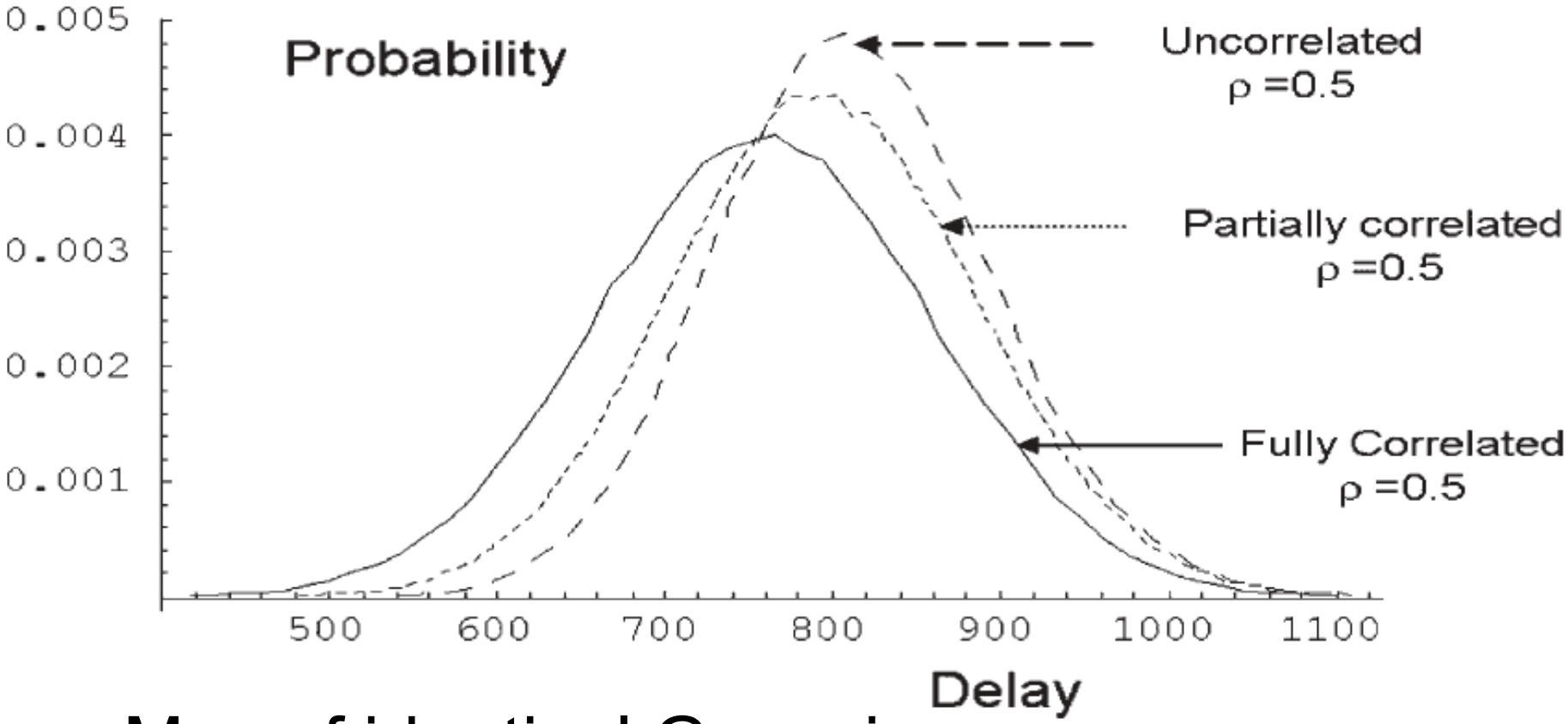


- Correlation
  - Physical on die
  - In path (reconvergent fanout)
    - Makes result conservative
      - Gives upper bound
      - Can compute lower



Graphics from: Noel Menezes (top) and Nikil Mehta (bottom)

Max of Gaussians with Correlation



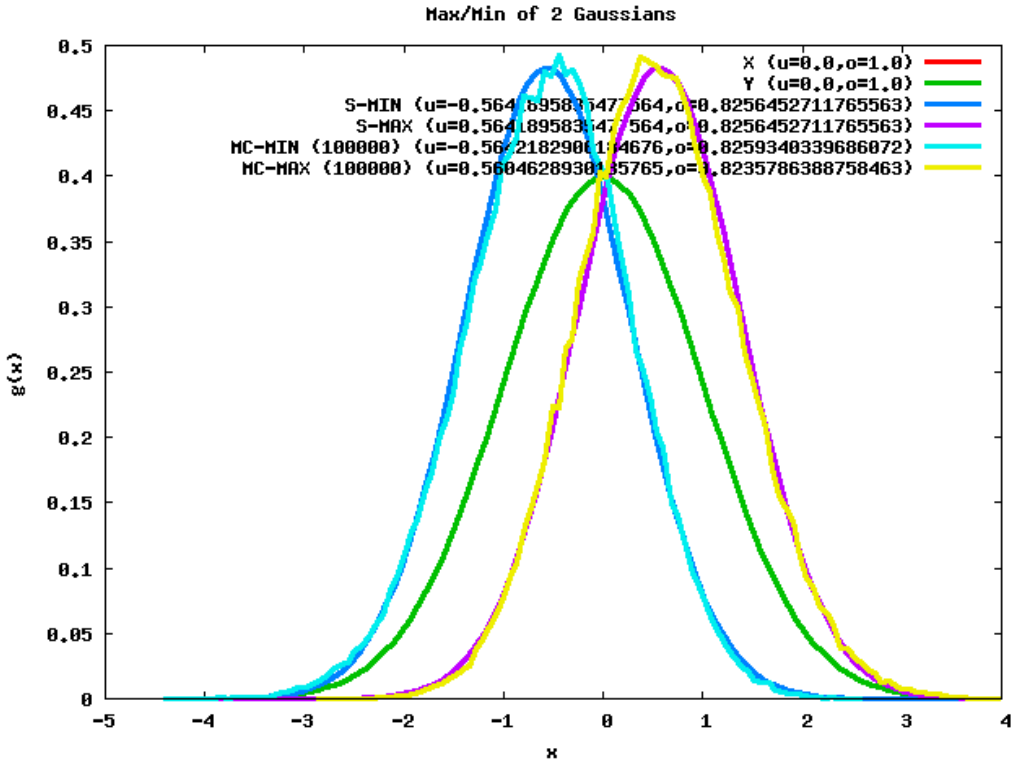
- Max of identical Gaussians

[Blaauw et al. TRCAD v27n4p589]

MAX of Two Identical Gaussians

- Given two identical Gaussians A and B with μ and σ
- Plug into equations
- E[MAX(A,B)] = $\mu + \sigma/(\pi)^{1/2}$
- VAR[MAX(A,B)] = $\sigma^2 - \sigma/\pi$

[Source: Nikil Mehta]



Extreme of correlated: is just the input Gaussian

SSTA vs. Monte Carlo Verification Time

TABLE II
MONTE CARLO VERSUS EinsStat COMPARISON

Test case	Gates	EinsStat CPU	Monte Carlo		
			Samples	Sequential CPU dd:hh:mm:ss	Parallel CPU dd:hh:mm:ss
1	18	1 sec.	100000	5:57	N/A
2	3042	2 sec.	100000	2:01:15:10	2:46:55
3	11937	7 sec.	10000	0:20:33:40	51:05
4	70216	59 sec.	10000	N/A	4:36:12

Source: IBM, TRCAD 2006

Using SSTA in FPGA CAD

[Slide composed by Nikil Mehta]

- Le Hei
  - FPGA2007
  - SSTA Synthesis, Place, Route
- Kia
  - FPGA2007
  - Route with SSTA

process variation settings (3σ)						
global spatial local	5.0% 5.0% 3.0%	10.0% 10.0% 6.0%	15.0% 15.0% 9.0%	20.0% 20.0% 12.0%	25.0% 25.0% 15.0%	30.0% 30.0% 18.0%
deterministic flow						
Tmean (ns) Tsigma (ns)	21.7 1.8	22.9 3.4	24.4 5.0	26.2 6.4	28.2 7.8	30.2 9.2
stochastic flow						
Tmean (ns)	20.3 (-6.5%)	21.5 (-6.2%)	23.0 (-5.8%)	24.8 (-5.5%)	26.7 (-5.3%)	28.6 (-5.1%)
Tsigma (ns)	1.6 (-6.6%)	3.1 (-7.5%)	4.6 (-8.1%)	5.9 (-8.2%)	7.2 (-8.1%)	8.5 (-8.0%)

Table 6: Comparison of mean delay and standard deviation between deterministic and stochastic flows under various process variation assumptions (based on the geometric mean of 20 MCNC designs).

Circuit	Delay Impr.(%)
ex5p	6.58
alu4	1.50
misex3	5.76
apex2	3.24
apex4	2.57
pdc	4.74
seq	4.37
des	3.73
spla	4.82
ex1010	1.83
frisc	2.84
elliptic	0.17
bigkey	0.35
s298	7.10
tseng	5.93
diffeq	4.16
dsip	7.37
s38417	7.56
s38584.1	5.43
clma	-1.17
Mean	**3.95**

Impact of SSTA in High-Level Synthesis

Design (#ops)	#ALU, #MUL	p_{clk} (ns)	Latency(cycles)		Reduction	Run time(s)
			LS[15]	HLS-tv(Y)		
DIFF (18)	3, 3	3.5	32	28 (94.5%)	12.5%	928
		4.0	29	24 (90.7%)	17.2%	930
		4.5	26	22 (93.2%)	15.4%	637
LATT (22)	3, 2	3.5	47	36 (94.3%)	23.4%	2122
		4.0	42	32 (94.3%)	23.8%	3325
		4.5	37	30 (90.2%)	18.9%	1207
AR (28)	2, 3	3.5	57	45 (93.9%)	21.1%	1241
		4.0	51	40 (93.9%)	21.6%	1534
		4.5	45	36 (90.8%)	20.0%	680
EWF (34)	2, 3	3.5	46	37 (93.6%)	19.6%	157
		4.0	42	34 (93.6%)	19.0%	367
		4.5	38	33 (91.5%)	13.2%	113
avg.				- **(92.9%)**	**18.8%**	

- Scheduling and provisioning
  - ALU/MUL σ=5% $t_{nominal}$

[Jung&Kim ICCAD2007]

Summary

- Nanoscale fabrication is a statistical process
- Delays are PDFs
- Assuming each device is worst-case delay is too pessimistic
  - Wrong prediction about timing
  - Leads optimization in wrong direction
- Reformulate timing analysis as statistical calculation
- Estimate the PDF of circuit delays
- Use this to drive optimizations

Big Ideas:

- Coping with uncertainty
- Statistical Reasoning and Calculation

Admin

- Reading for Monday on canvas
- Milestone Thursday