ESE 568: Mixed Signal Circuit Design and Modeling

Lec 1: August 28, 2019

Introduction and Overview

Where I come from

- Analog VLSI Circuit Design (analog design)
- Convex Optimization (system design)
  - System Hierarchical Optimization
- Biomedical Electronics
- Biometric Data Acquisition (signal processing)
  - Compressive Sampling
- ADC Design (mixed signal)
- Low Energy Circuits (digital design)
  - Adiabatic Charging

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- ADC Design (mixed signal)
- Low Energy Circuits (digital design)
  - Adiabatic Charging
- CIRCUITS, CIRCUITS, CIRCUITS

Getting to Know You

- Cadence?
- ESE 419/572?
- Circuit knowledge

- Diagnostic Survey/Quiz in Canvas
  - Due Friday, not graded

Getting to Know You

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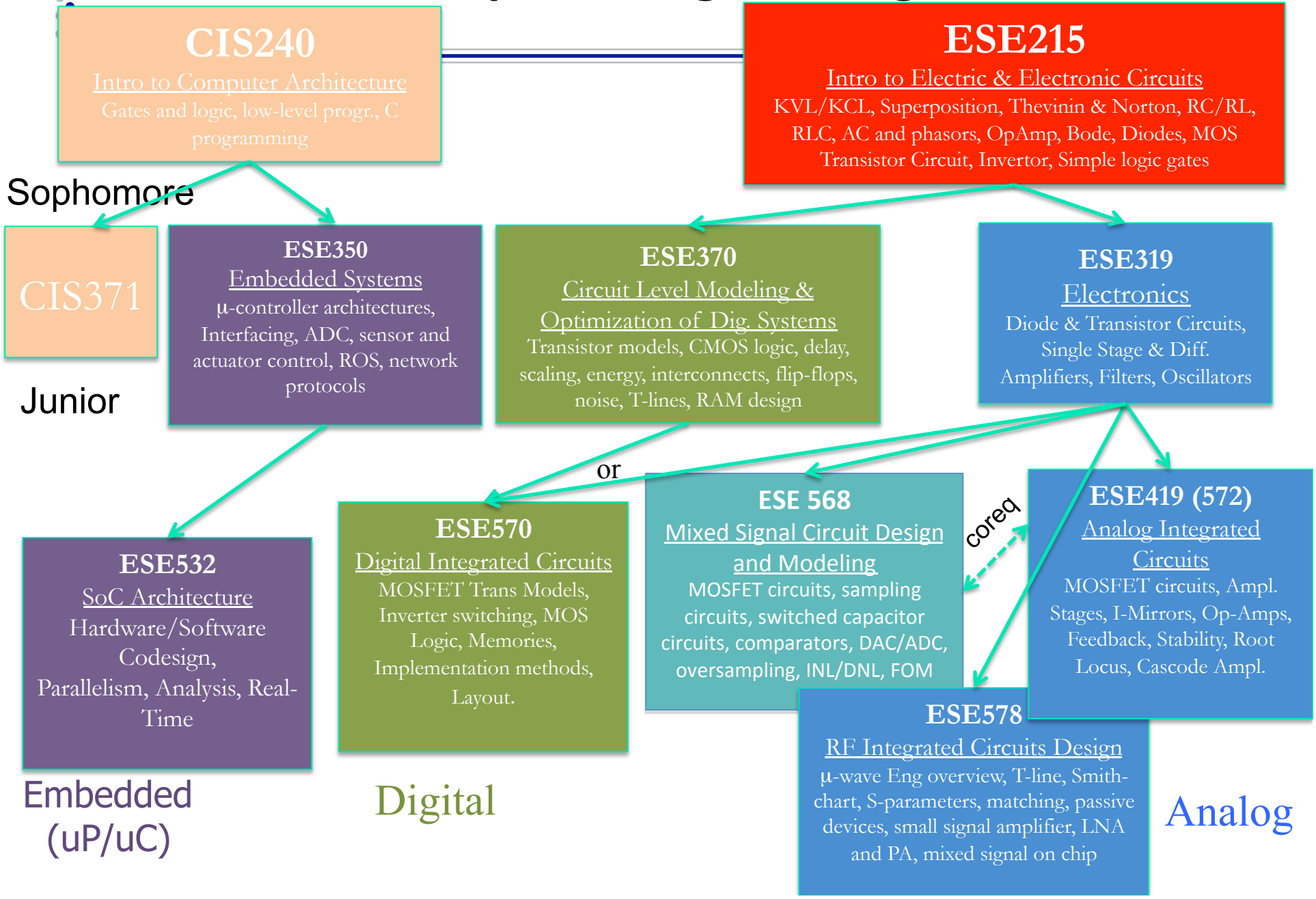
- ESE 419/572?
- Circuit knowledge

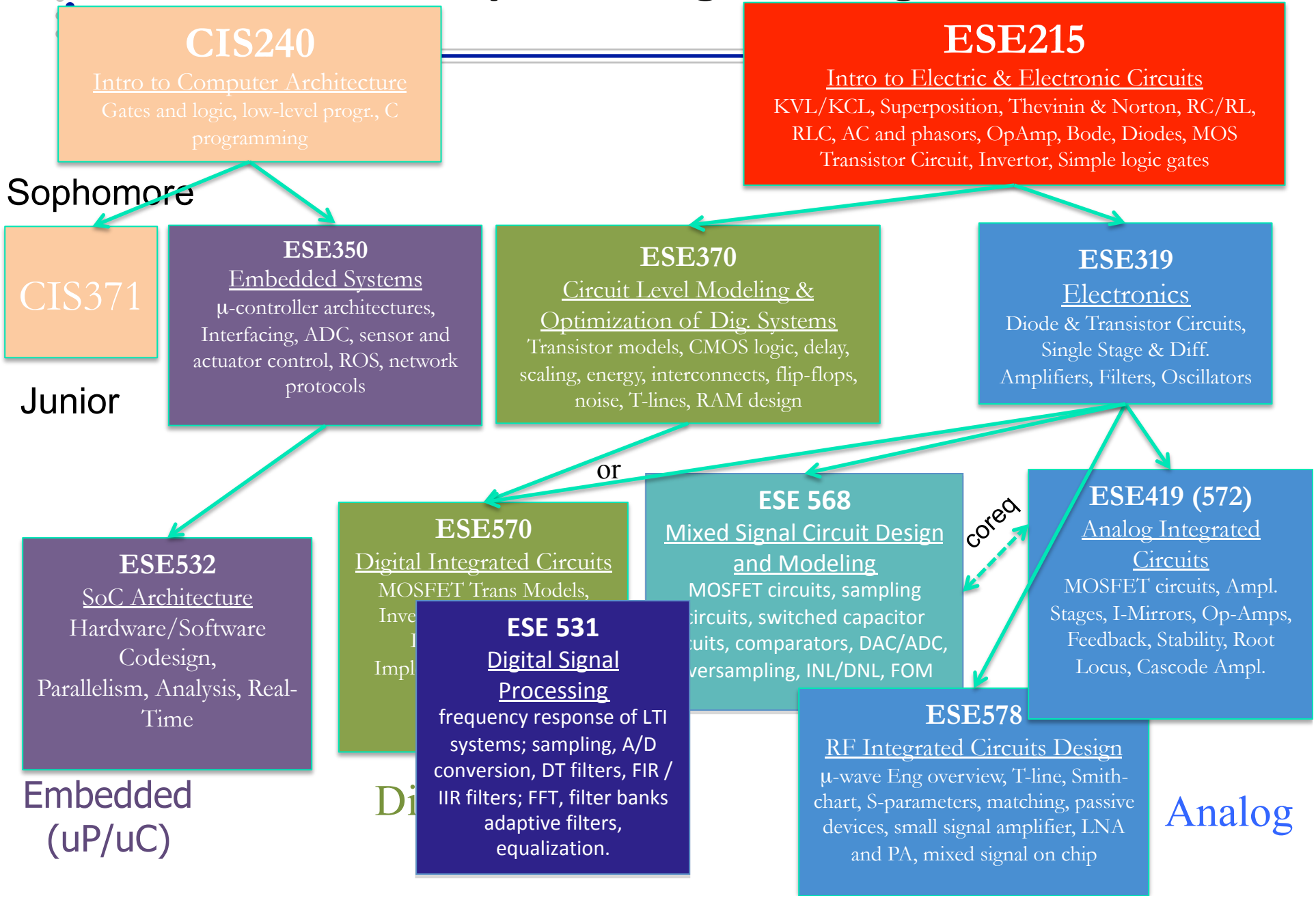
- Diagnostic Survey/Quiz in Canvas
  - Due Friday, not graded

- WARNING: You should have already take ESE 419/572 or be taking it at the same time as this class

Circuits and Computer Engineering



Circuits and Computer Engineering



Lecture Outline

- Course Topics Overview
- Course Structure
- Course Policies
- Course Content
- Mixed Signal Systems
- Course Objectives

Course Topics Overview

- Ideal Sampling and Quantization
- Static and Spectral Performance Metrics
- Sampling Circuits
- Switched Capacitor Circuits
- Comparators, DACs
- SAR ADCs
- Flash ADCs
- Pipeline ADCs
- Time Interleaving, Oversampling
- Other Converter Topologies
- Industry Trends
- F(igure)O(f)M(erit)

Course Topics Overview

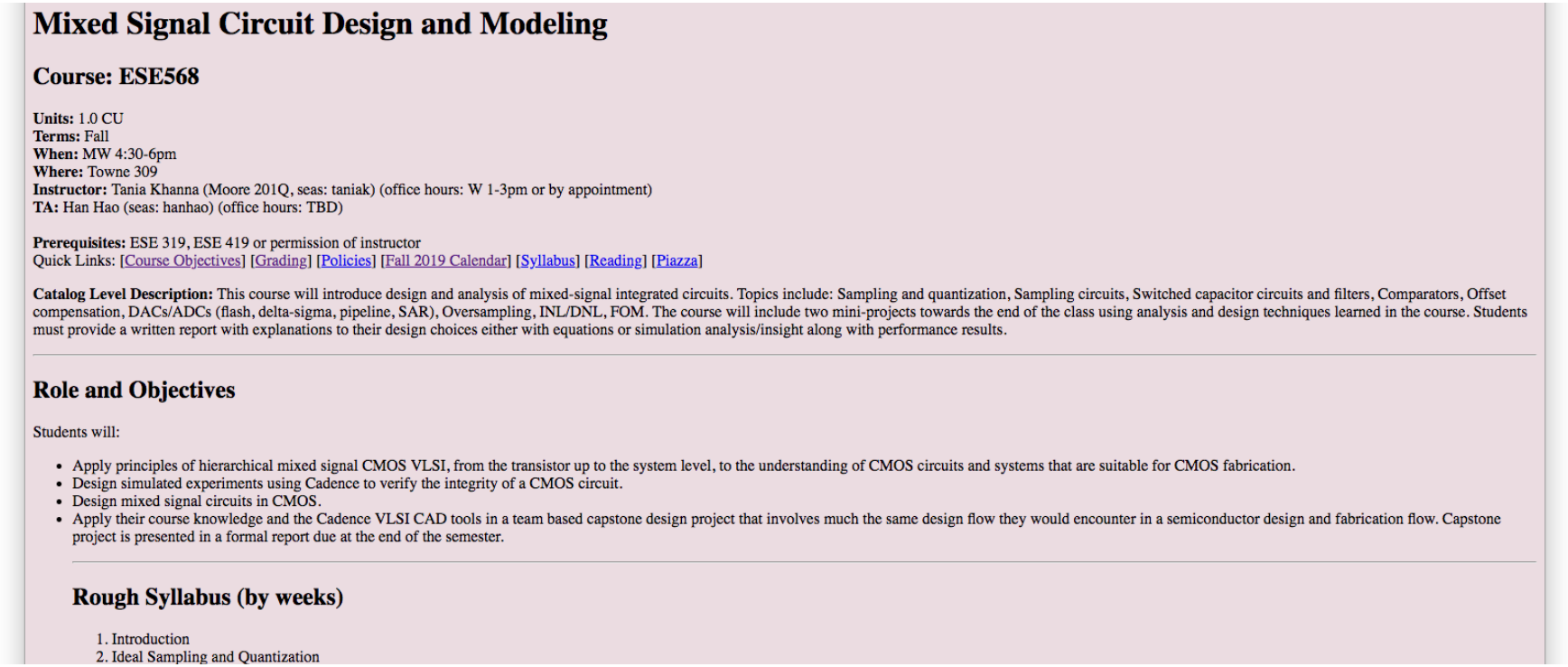
- In other words…

- ADCs, ADCs, ADCs

- Analysis, Design, and Testing

Course Structure

- MW Lecture, 4:30-6:00pm in Towne 309
  - Start 5 minutes after, end 5 minutes early (~80min)
- Website (http://www.seas.upenn.edu/~ese568/)



Mixed Signal Circuit Design and Modeling

Course: ESE568

Units: 1.0 CU
Terms: Fall
When: MW 4:30-6pm
Where: Towne 309
Instructor: Tania Khanna (Moore 201Q, seas: taniak) (office hours: W 1-3pm or by appointment)
TA: Han Hao (seas: hanhao) (office hours: TBD)

Prerequisites: ESE 319, ESE 419 or permission of instructor
Quick Links: [Course Objectives] [Grading] [Policies] [Fall 2019 Calendar] [Syllabus] [Reading] [Piazza]

Catalog Level Description: This course will introduce design and analysis of mixed-signal integrated circuits. Topics include: Sampling and quantization, Sampling circuits, Switched capacitor circuits and filters, Comparators, Offset compensation, DACs/ADCs (flash, delta-sigma, pipeline, SAR), Oversampling, INL/DNL, FOM. The course will include two mini-projects towards the end of the class using analysis and design techniques learned in the course. Students must provide a written report with explanations to their design choices either with equations or simulation analysis/insight along with performance results.

Role and Objectives

Students will:

- Apply principles of hierarchical mixed signal CMOS VLSI, from the transistor up to the system level, to the understanding of CMOS circuits and systems that are suitable for CMOS fabrication.
- Design simulated experiments using Cadence to verify the integrity of a CMOS circuit.
- Design mixed signal circuits in CMOS.
- Apply their course knowledge and the Cadence VLSI CAD tools in a team based capstone design project that involves much the same design flow they would encounter in a semiconductor design and fabrication flow. Capstone project is presented in a formal report due at the end of the semester.

Rough Syllabus (by weeks)

1. Introduction
2. Ideal Sampling and Quantization

Course Structure

- MW Lecture, 4:30-6:00pm in Towne 309
  - Start 5 minutes after, end 5 minutes early (~80min)
- Website (http://www.seas.upenn.edu/~ese568/)
  - Course calendar is used for all handouts (lectures slides, assignments, and readings)
  - Canvas used for assignment submission and grades
  - Piazza used for announcements and discussions

Course Structure

- Course Staff (complete info on course website)
- Instructor: Tania Khanna
  - Office hours – Wednesday 1-3:00 pm or by appointment
  - Email: taniak@seas.upenn.edu
    - Best way to reach me
- TAs: Han Hao
  - Office Hours – TBD
- Piazza for questions

Course Structure

- Lectures
  - Statistically speaking, you will do better if you come to lecture
  - Better if interactive, **everyone** engaged
  - Review/Q&A Lectures
- Textbook
  - *Analog Integrated Circuit Design*, Carusone, Johns, and Martin, 2nd edition
    - Great reference text with lots of detail
  - Additional Reference:
    - *Design of Analog CMOS Integrated Circuits*, Behzad Razavi, 1st edition

Course Structure

- Cadence
  - Schematic simulation (SPECTRE simulator)
    - Design, analysis and test
  - No Layout
  - Will get started with it in HW 2

Course Structure - Assignments/Exams

- Diagnostic Survey/Quiz in Canvas
  - Complete by Friday this week, already out
- Homework – 1 week long (5 total) [35%]
  - Due Sundays at midnight
  - No late assignments, no grace period
- Midterm exam [25%]
- 3 Projects – 2-3 weeks long [40%]
  - Design oriented
  - Do well on the projects → Do well in the class

Course Structure - Assignments/Exams

ESE568 Fall 2019 Working Schedule

Wk	Lect.	Date		Lecture	Slides	Due	Reading
1	1	8/28	W	Introduction and Overview	[lec1] [lec1_6up]		review course web page completely
		8/30	F			Diagnostics Quiz	
2		9/2	M	Labor Day			
	2	9/4	W	MOS Models: Devices and Large Signal			1.2
		9/8	Su			HW 1 HW1.xls	
3	3	9/9	M	MOS Models: Small Signal, CMOS Subcircuits			3.1-3.3, 3.7-3.8
	4	9/11	W	Differential Amplifier, Basics of Opamp Design			6.1-6.2
		9/15	Su			HW2	
4	5	9/16	M	Basic Opamp Design			6.4-6.7
	6	9/18	W	Basic Opamp Design (con't), Advanced Opamp Design			9.1, 9.3
		9/22	Su			HW3	
5	7	9/23	M	Sampling, Reconstruction, Quantization, Static Performance Metrics			15.1-15.3
	8	9/25	W	Static Performance Metrics			15.1-15.3
		9/29	Su				
6	9	9/30	M	Spectral Performance Metrics			15.5
	10	10/2	W	Sampling Circuits			11.1-11.2 14.4
		10/6	Su			Proj1	
7	11	10/7	M	Switched Capacitor Circuits			14.1-14.2
	12	10/9	W	Comparators			10.1-10.2, 10.4
		10/13	Su			HW4	
8	13	10/14	M	Latch Comparators			10.1-10.2, 10.4
		10/16	W	Review and Q&A			17.5
		10/20	Su			HW5	
9	14	10/21	M	Flash ADCs, Pipeline ADCs			17.5, 17.4
	15	10/23	W	Pipeline ADCs (con't)			17.4
10		10/28	M	MIDTERM EXAM in class			
	16	10/30	W	Pipeline ADCs (con't)			17.4
11	17	11/4	M	SAR ADCs			17.2-17.3
	18	11/6	W	Nyquist Rate DACs, Interleaved ADCs			18.1-18.2.1
12	19	11/11	M	Oversampling, Delta Sigma ADC/DACs			18.3
		11/14	W	Review and Q&A			
		11/18	Su			Proj2	
13	20	11/18	M	Data Converter Testing			15.5-15.6

Course Policies

See web page for full details

- Turn homework in Canvas
  - Anything handwritten/drawn must be clearly legible
  - Submit CAD generated figures, graphs, results when specified
  - NO LATE HOMEWORKS!
- Individual work (except projects)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help

Course Content

- Analog IC basics review [3 weeks]
- Data converter basics [1.5 week]
- Switched Capacitor Circuits [2 weeks]
- Data converter [7 weeks]
  - Architectures
  - Testing
  - Trends
- Frequency synthesis/layout [1.5 week]

Course Content

- Analog IC basics review [3 weeks]
  - Microelectronics review
    - MOS models
    - CMOS subcircuits
    - Opamp design
    - Noise models
  - **Project 1**: Design opamp

Course Content

- Data converter basics [1.5 week]
  - Signal abstraction level
    - Reconstruction and Quantization
      - Going from analog to digital and vice versa
    - Static and Spectral Perf. Metrics
      - VTC
      - INL/DNL
      - SNR/SNDR
      - ENOB, etc.

Course Content

- Switched Capacitor Circuits [2 weeks]
  - Sampling Circuits
    - Ideal sampling
    - Sampling non-idealities
  - Switch Capacitor Circuits
    - T/H, Differance amps, Integrators
  - Comparators
    - Opamp comparators, latch comparators
  - Analyze and compare given comparator designs
  - **Project 2**: Design Sample and Hold circuit

Course Content

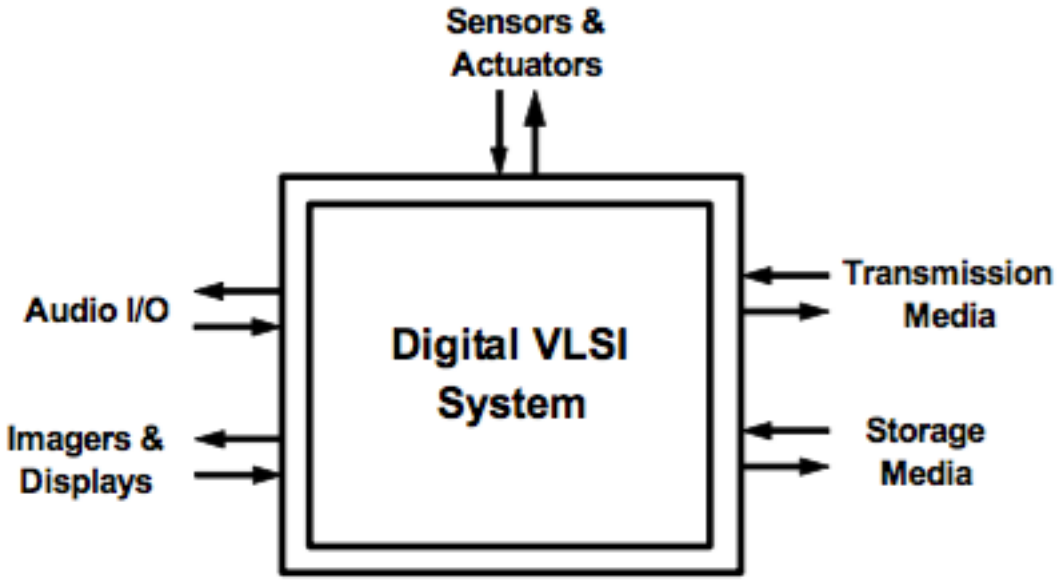
- Data converter architectures [7 weeks]
  - ADC architectures
    - Nyquist ADCs
      - Flash, Pipeline, SAR
    - Nyquist DACs
      - Unit-element, Binary weighted
    - Oversampling (non-Nyquist)
      - Interleaved ADCs
      - Delta-Sigma ADC/DACs
  - Data Converter Testing
    - Strategies in simulation and lab settings
    - Performance measure (FOM)
  - Performance trends and limits
  - Project 3: Design and characterize ADCs!!

Course Content

- Frequency synthesis/Layout [1.5 week]
  - VCOs
  - PLL/DLLs
  - Layout Techniques
    - Floor planning
    - Common centroid
    - Decoupling

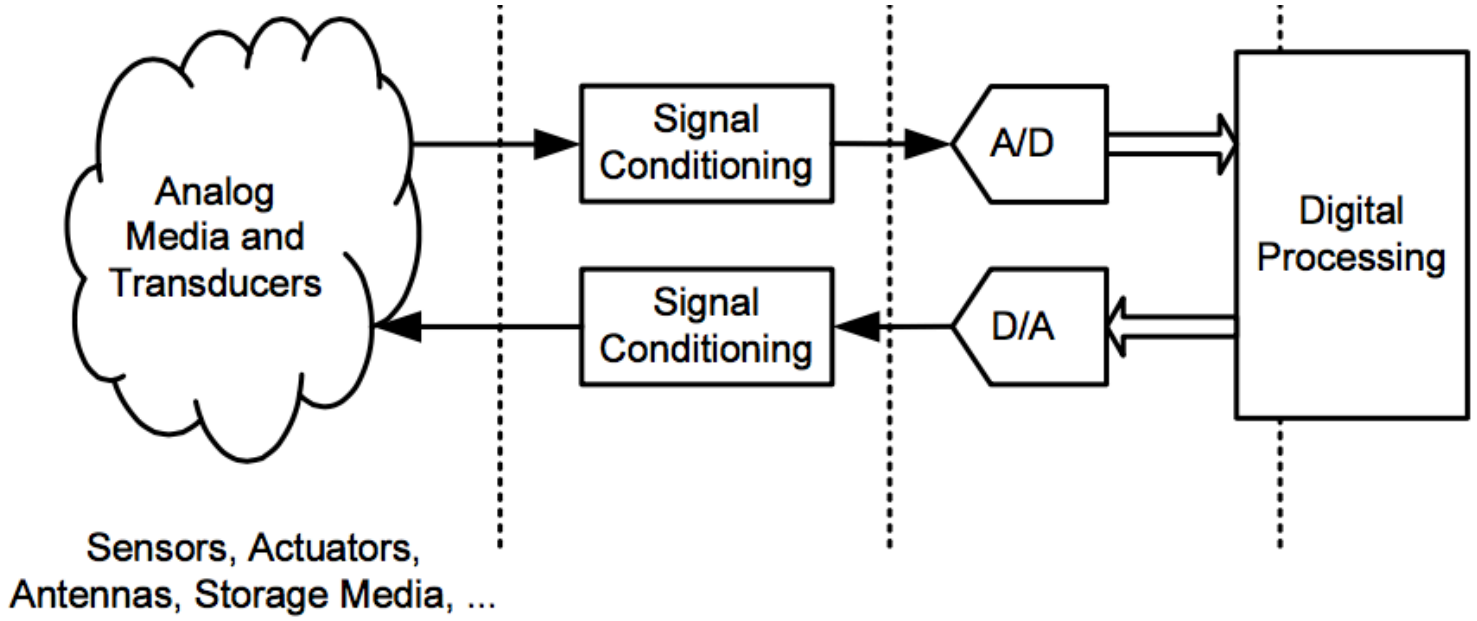
Mixed Signal VLSI

ADC Design Motivation

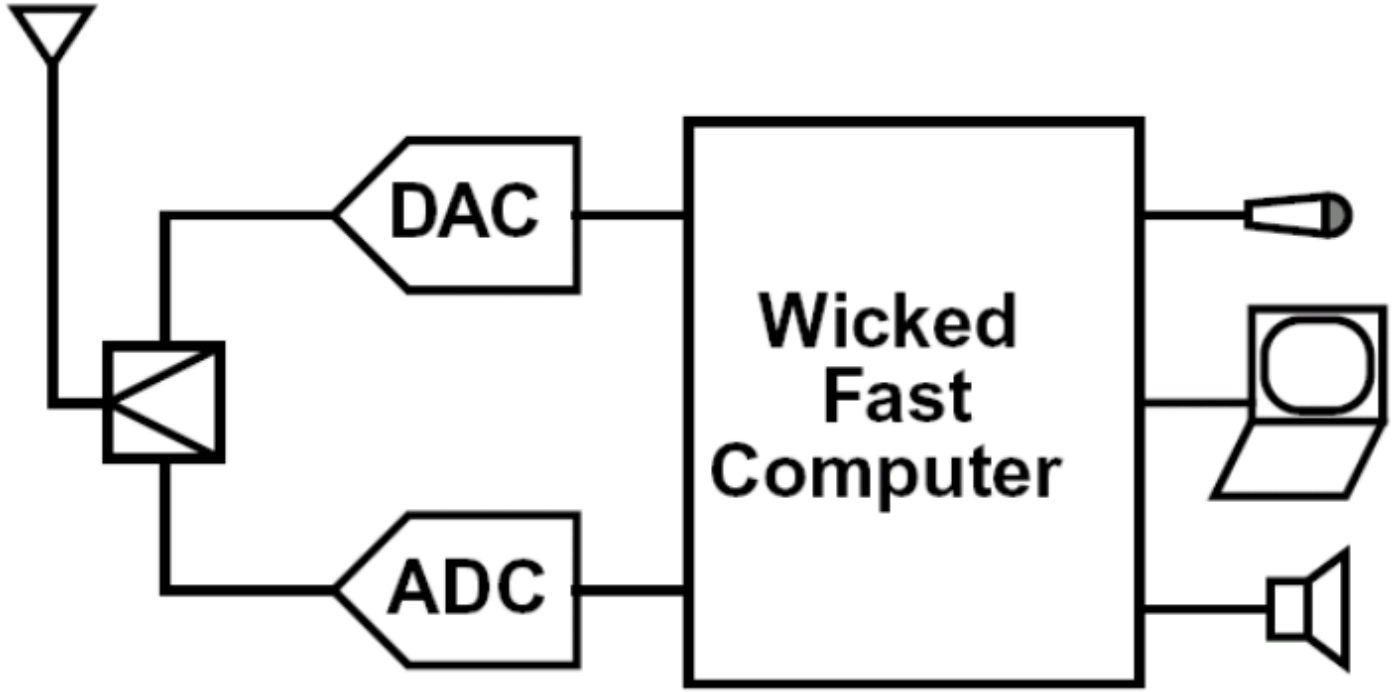


- Information is increasingly being stored, processed and communicated in digital form
- Since physical signals are analog in nature, we need A/D and D/A conversion interfaces

Mixed Signal System

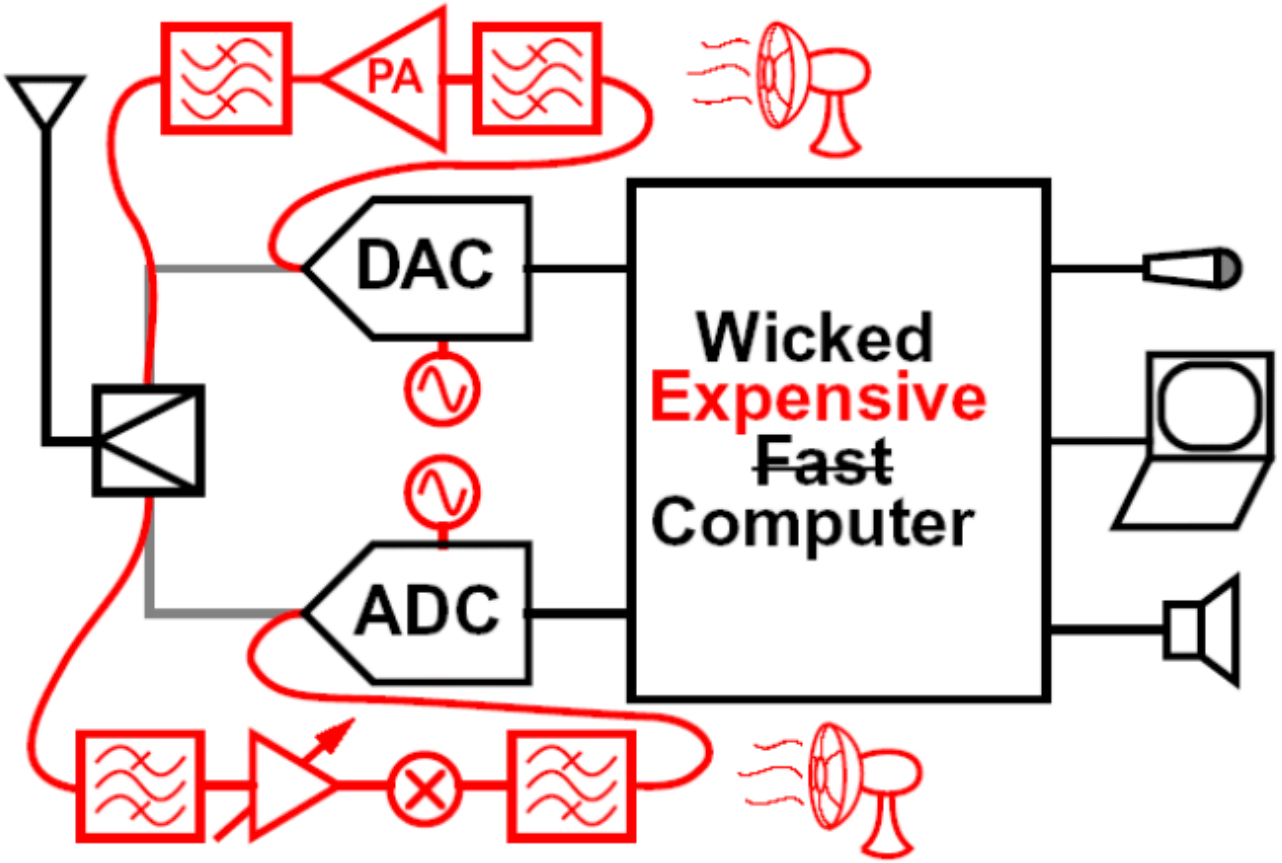


Software Radio Vision



[Schreier, "ADCs and DACs: Marching Towards the Antenna," GIRAFE workshop, ISSCC 2003]

Software Radio Reality



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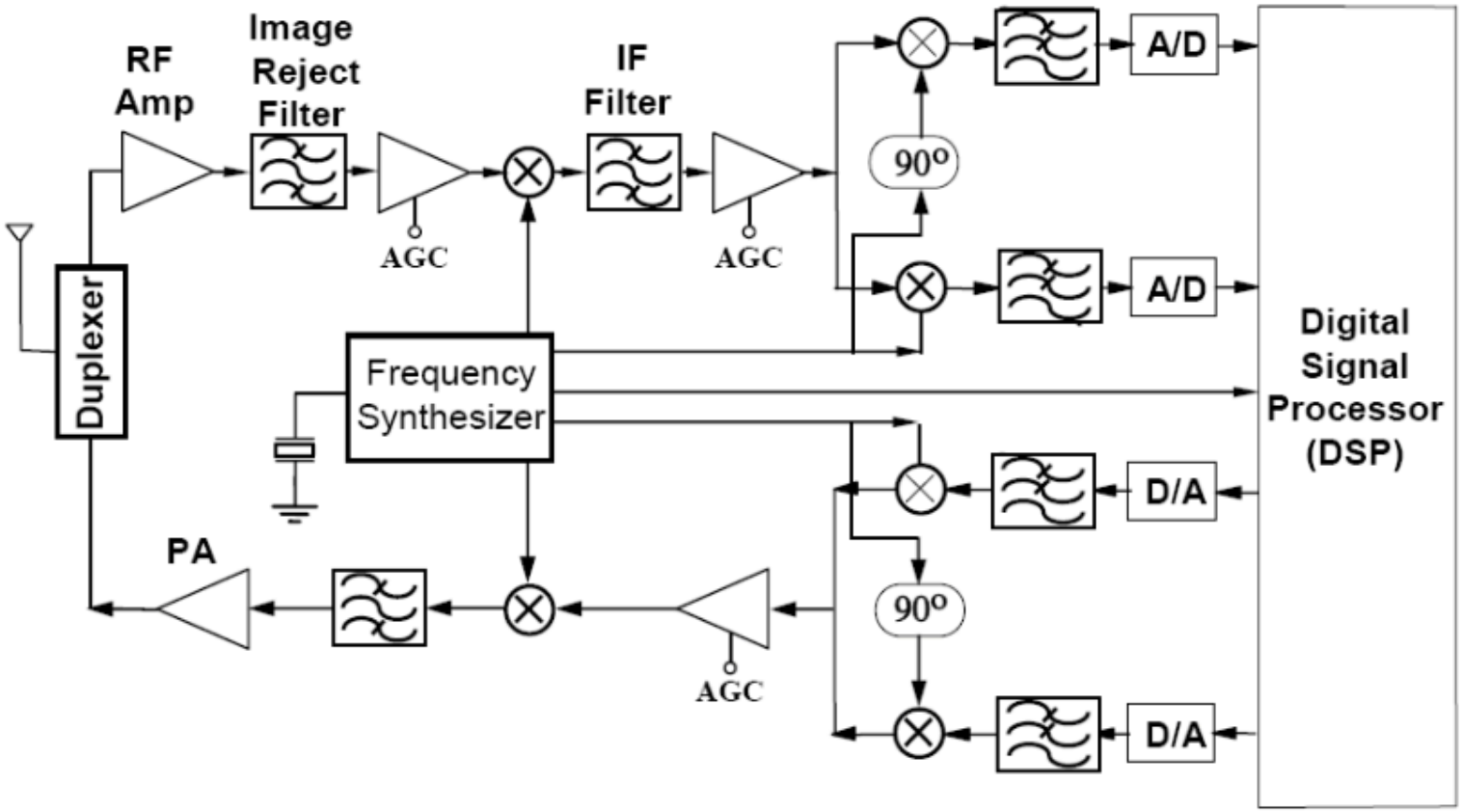
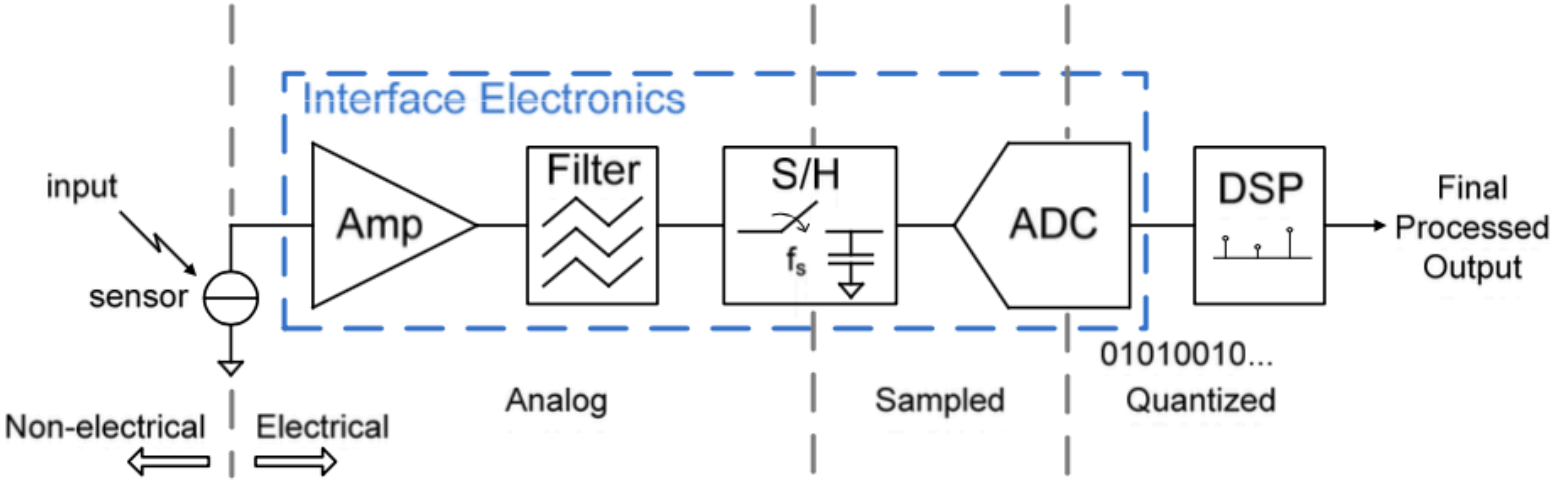
Example: Cell Phone

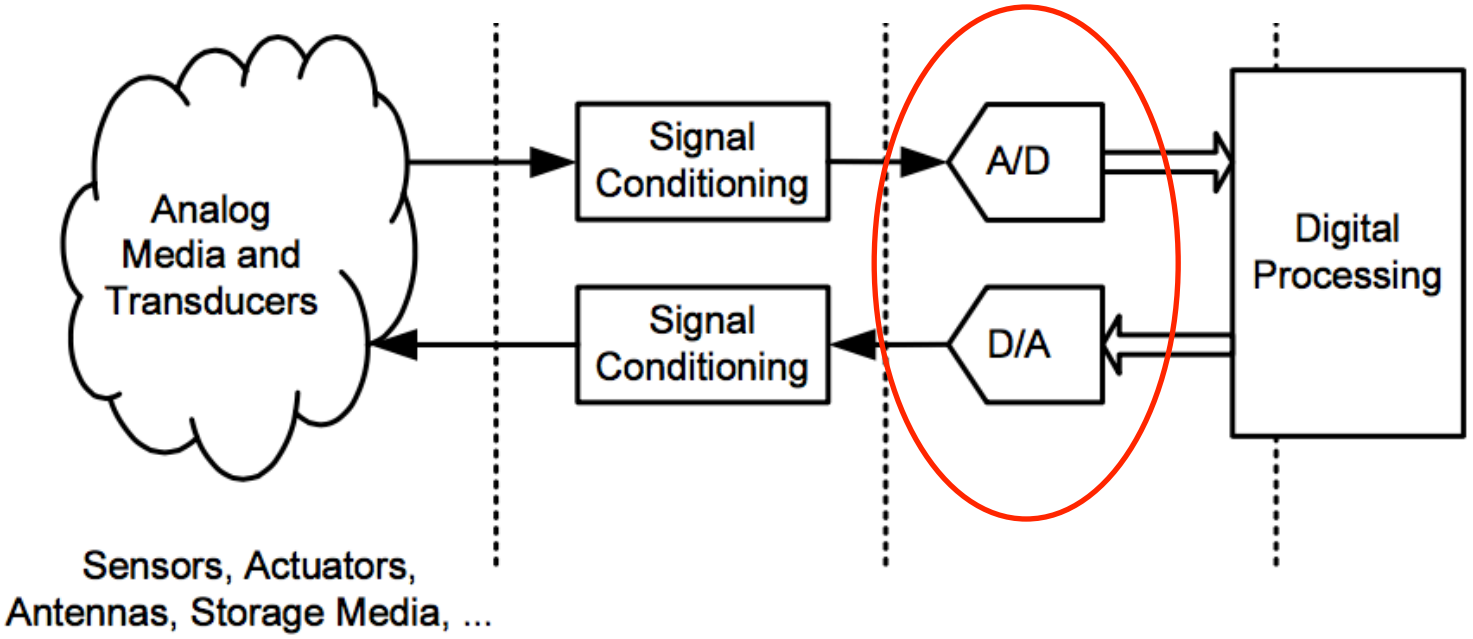


Canonical Sensing System

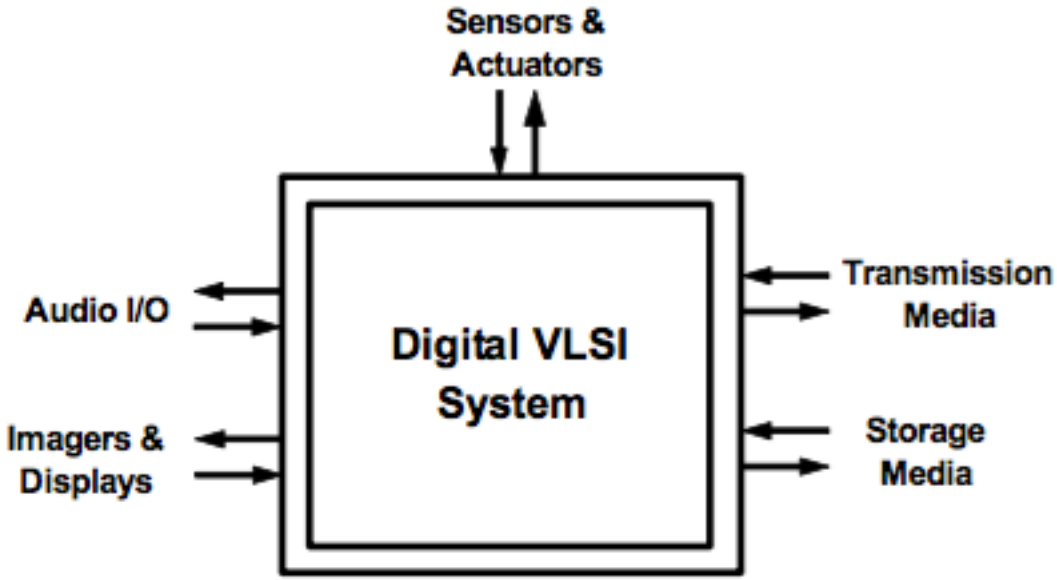


- Front-end amplification boosts the sensor's signal above the noise floor of the interface electronics
- Filtering rejects interference, noise, provides antialiasing
- System level optimization is needed
  - Don't want to waste power, money, area, accuracy, etc.

Mixed Signal System



ADC Design Motivation



- Information is increasingly being stored, processed and communicated in digital form
- Since physical signals are analog in nature, we need A/D and D/A conversion interfaces

ADC Design Motivation (con't)

- Benefits of digital signal processing
  - Reduced sensitivity to "analog" noise
  - Enhanced functionality and flexibility
  - Amenable to automated design & test
  - Direct benefit from the scaling of VLSI technology – "Arbitrary" precision
- Issues
  - Data converters are difficult to design
    - Especially due to ever-increasing performance requirements (eg. mobility, use models, and size)
  - Data converters often present a performance bottleneck
    - Speed, resolution or power dissipation of the A/D or D/A converter can limit overall system performance, especially in the case of small mobile devices

A/D Converter (1954)

- 19" × 15" × 26"
- 150 lbs
- 500W
- $8,500.00

Courtesy,
Analogic Corporation

Figure 4.3: *1954 "DATRAC" 11-bit, 50-kSPS SAR ADC Designed by Bernard M. Gordon at EPSCO*

http://www.analog.com/library/analogDialogue/archives/39-06/data_conversion_handbook.html

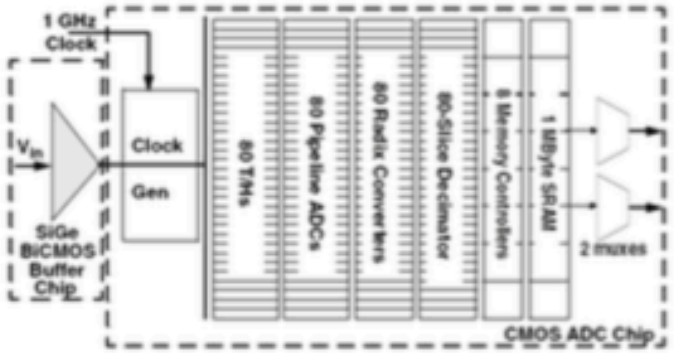
Applications

- Consumer electronics
  - Audio, TV, Video
  - Digital Cameras
  - Automotive control
  - Appliances
  - Toys
  - MEDICAL ELECTRONICS
- Communications
  - Smart Phones
  - WirelessTransceivers
  - Routers/Modems

Applications (con't)

- Computing and Control
  - Storage media
  - Sound Cards
  - Data acquisition cards
- Instrumentation
  - Lab bench equipment
  - Semiconductor test equipment
  - Scientific equipment
  - Medical equipment

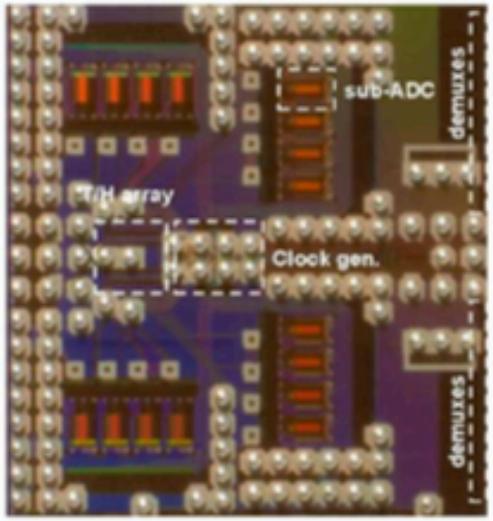
Example 1



[Poulton, ISSCC 2003]

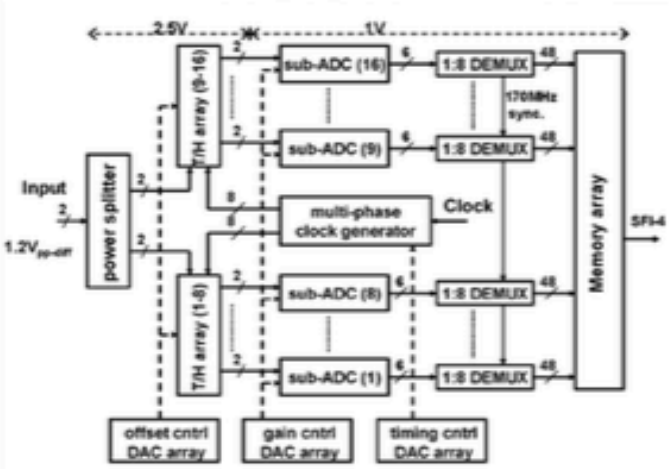
- High performance digital oscilloscopes rely on extremely high performance ADCs
- Example
  - 20 GSample/s, 8-bit ADC
  - 10 W Power dissipation

Example 2



Packaged ADC performance

Resolution	6b
Conversion rate	0.1 - 24GS/s
Input range	$1.2V_{pp-diff}$
ENOB average cal / cal each freq	 4.2/4.8, F_{in}= 8GHz 3.6/4.1, F_{in}= 12GHz
SFDR	40dB @ 8GHz 36dB @ 12GHz
Power	1.2W @ 1V and 2.5V
ADC core	4 x 4 mm^2
Process	90nm CMOS



- Schvan, ISSCC 2008
- Time interleaved architecture using 160 (!) SAR ADCs for optical networks

Example 3

- A typical cell phone contains:
  - 4 Rx ADCs
  - 4 Tx DACs

  } Dual Standard, I/Q

  - 3 Auxiliary ADCs
  - 8 Auxiliary DACs

  } Audio, Tx/Rx power control, Battery charge control, display, ...

- A total of 19 data converters!

Example 3

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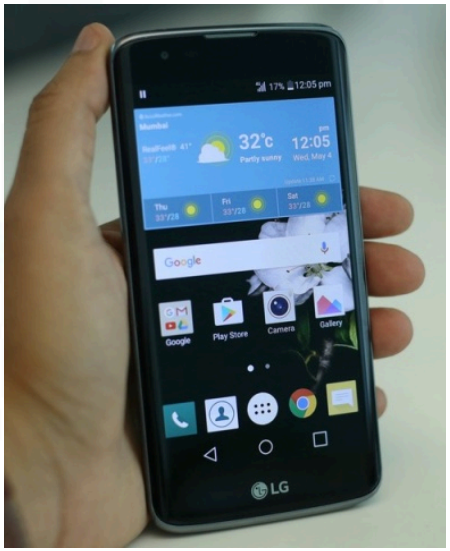
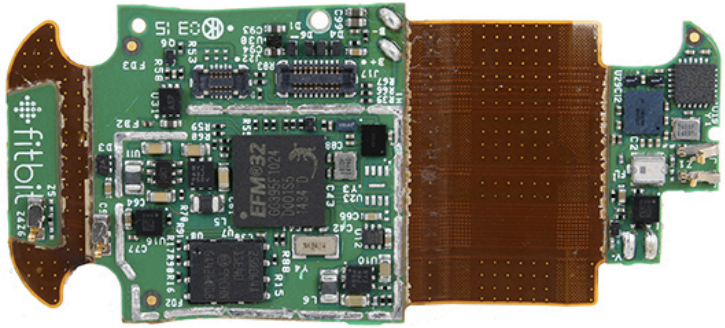


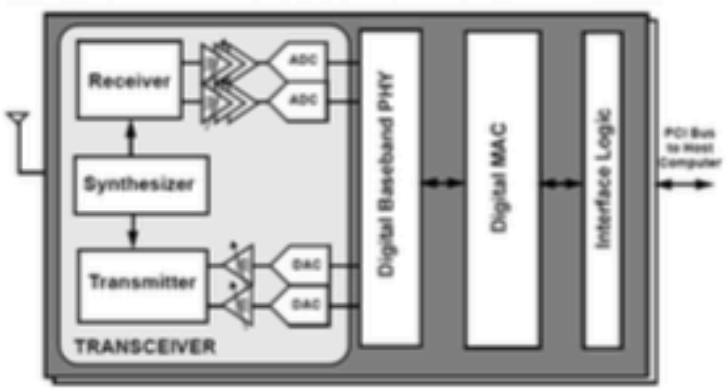
Even more with smartphones --
~15 ADC/DACs in Audio codec chip alone

Example 4

- Fitbit Surge
  - Microcontroller Solution (32-Bit ARM Cortex-M3)
  - Successive Approximation Register (SAR) architecture
  - 8 channel, 12-bit, 1Ms/s



Example 5

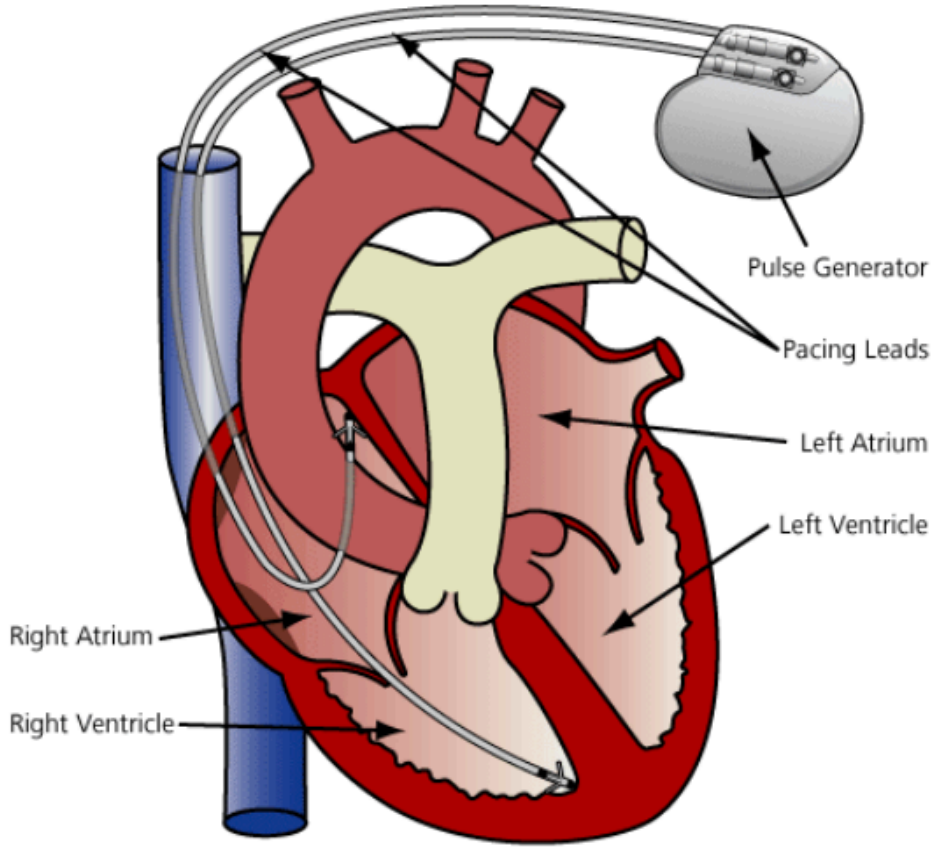


[Mehta, ISSCC2005]

- Low-cost, single chip solutions require embedded data conversion
- Example: 802.11g Wireless LAN chip
  - 2x 11-bit DAC, 176 MSamples/s
  - 2x 9-bit ADC, 80 MSamples/s

Example 6 – Cardiac Pacemaker System

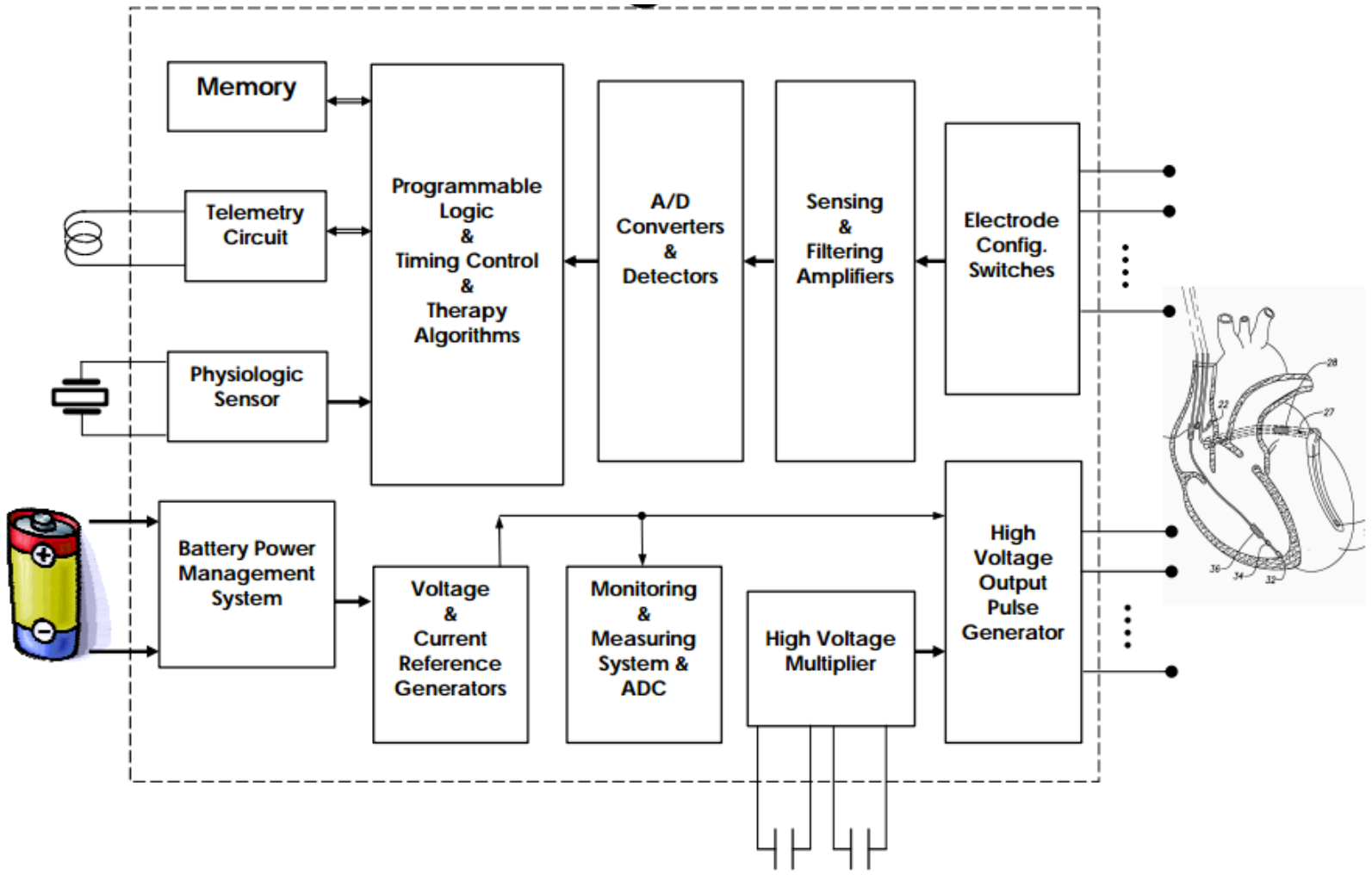
ST. JUDE MEDICAL | Global Leadership in Medical Technology



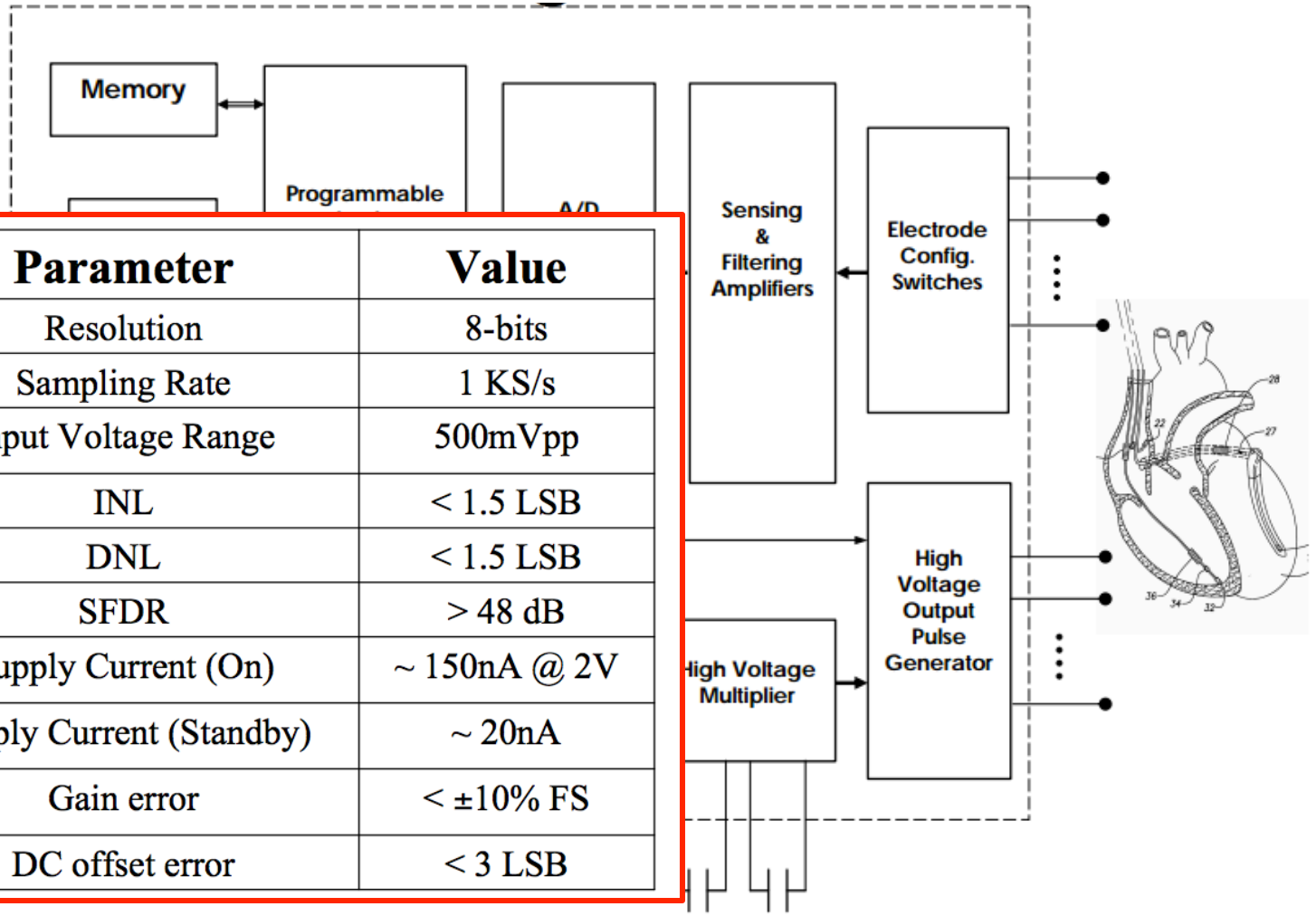
2 inch

Picture of an actual Implantable Pacemaker

Example 6 – Cardiac Pacemaker System

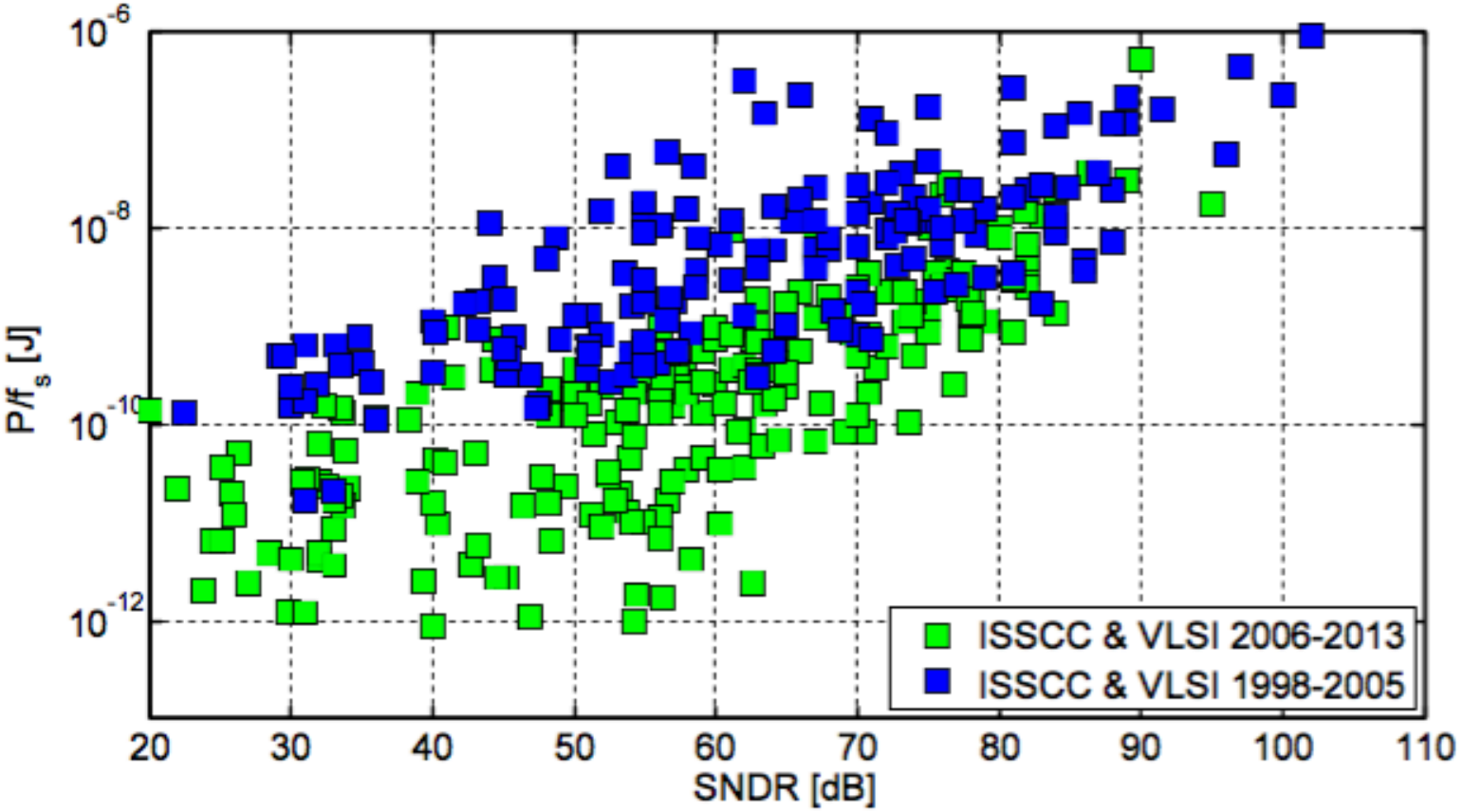


Example 6 – Cardiac Pacemaker System



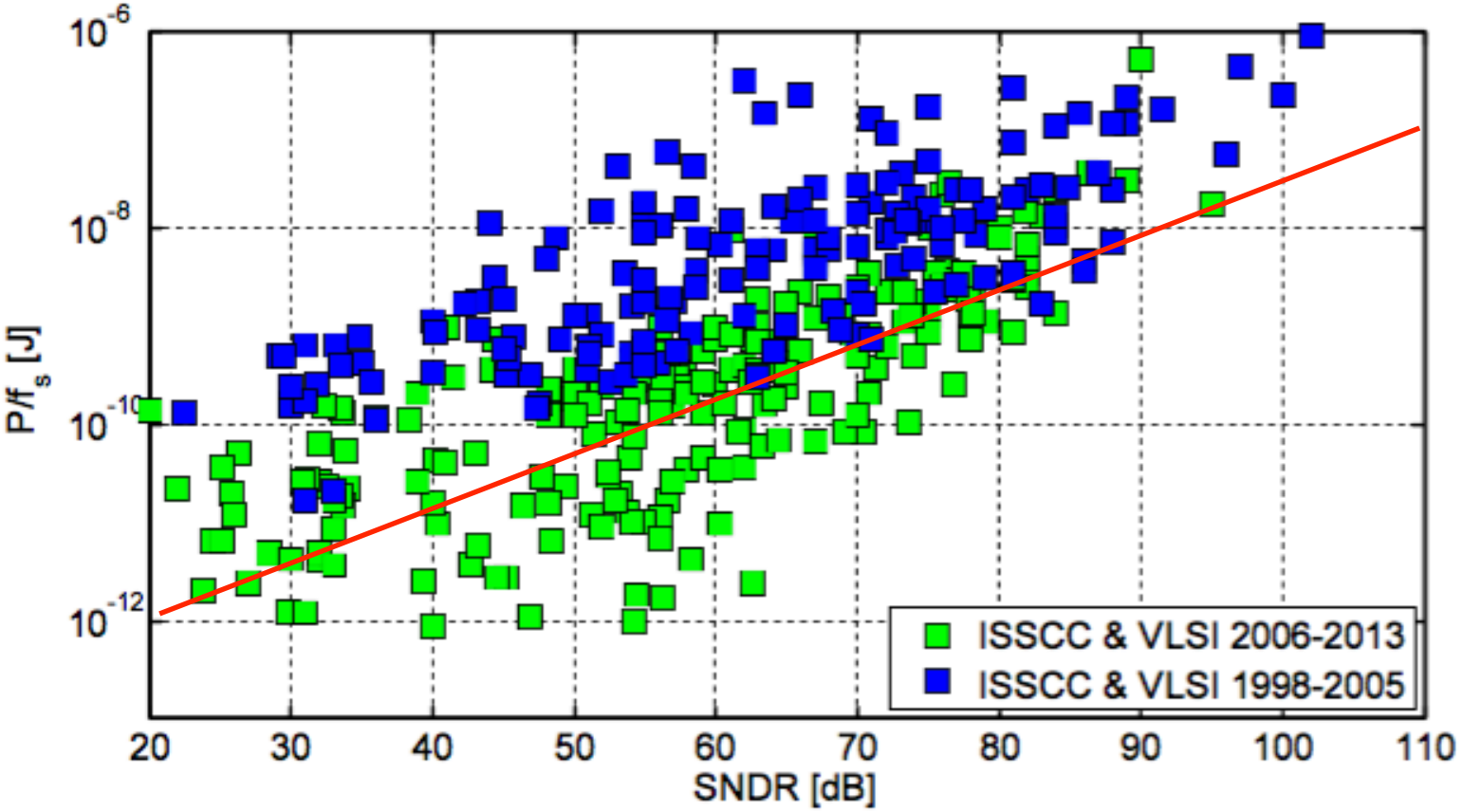
Parameter	Value
Resolution	8-bits
Sampling Rate	1 KS/s
Input Voltage Range	500mVpp
INL	< 1.5 LSB
DNL	< 1.5 LSB
SFDR	> 48 dB
Supply Current (On)	~ 150nA @ 2V
Supply Current (Standby)	~ 20nA
Gain error	< ±10% FS
DC offset error	< 3 LSB

ADC Design Trend



B. Murmann, "ADC Performance Survey 1997-2013," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

ADC Design Trend



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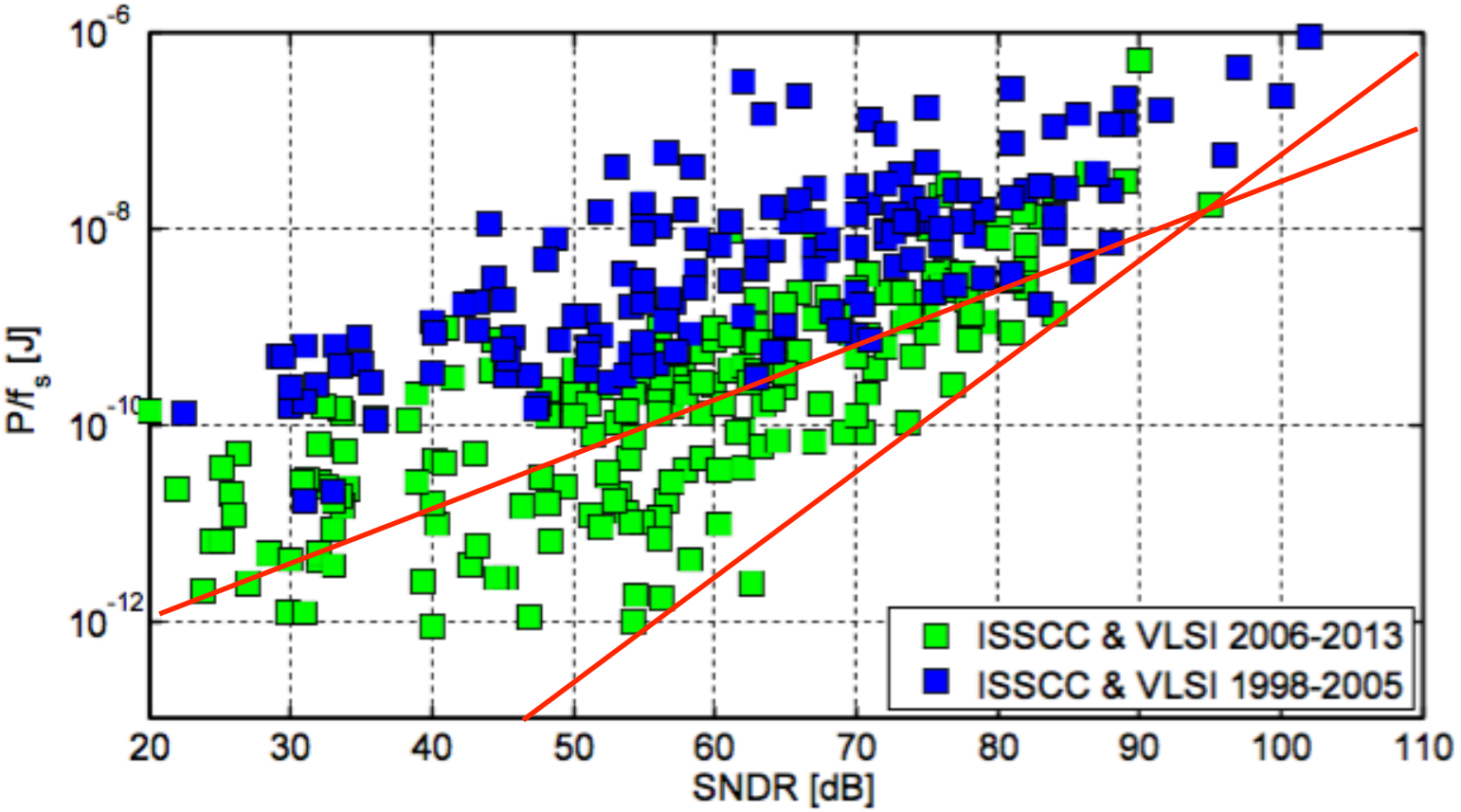
ADC Design Trend



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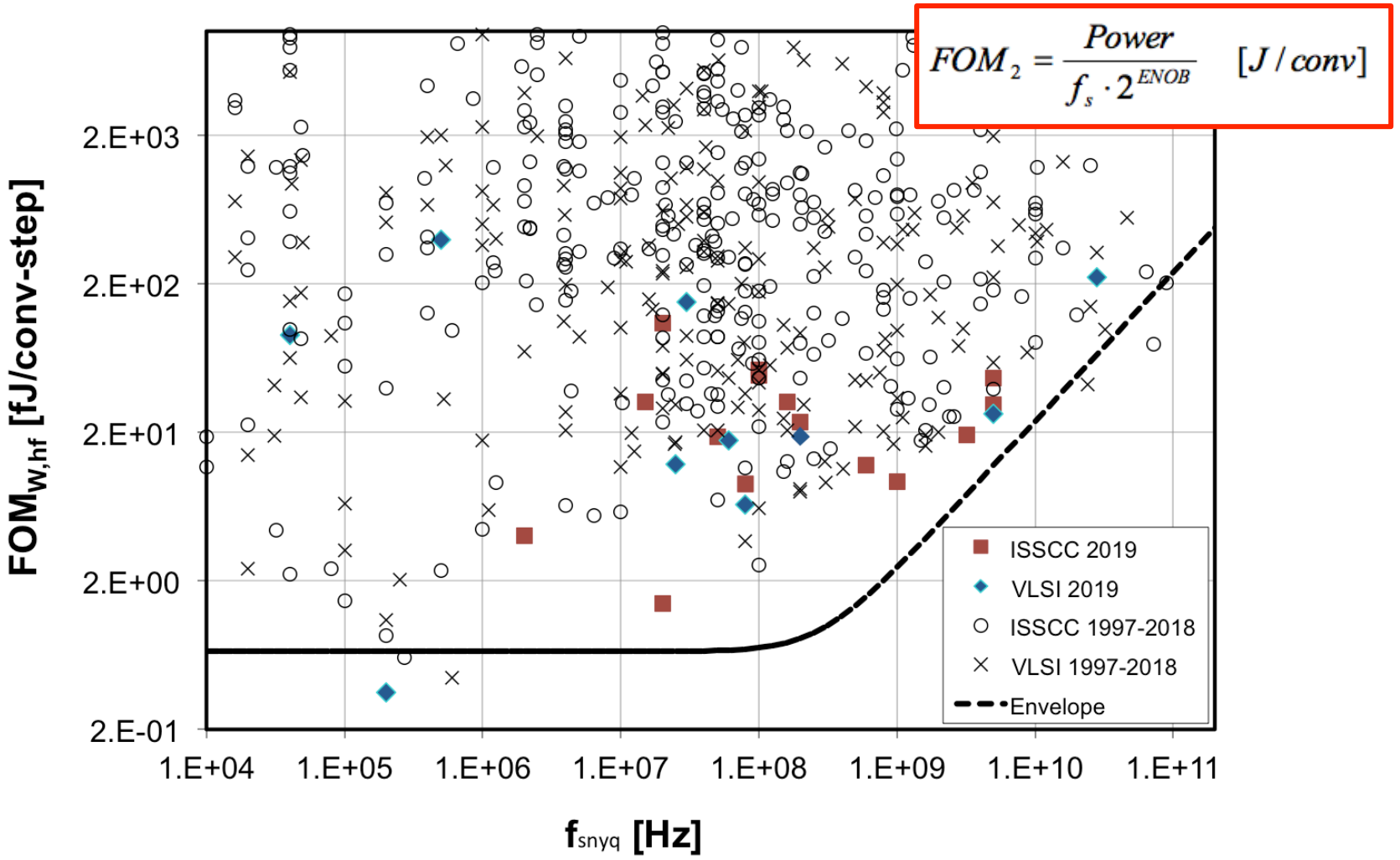
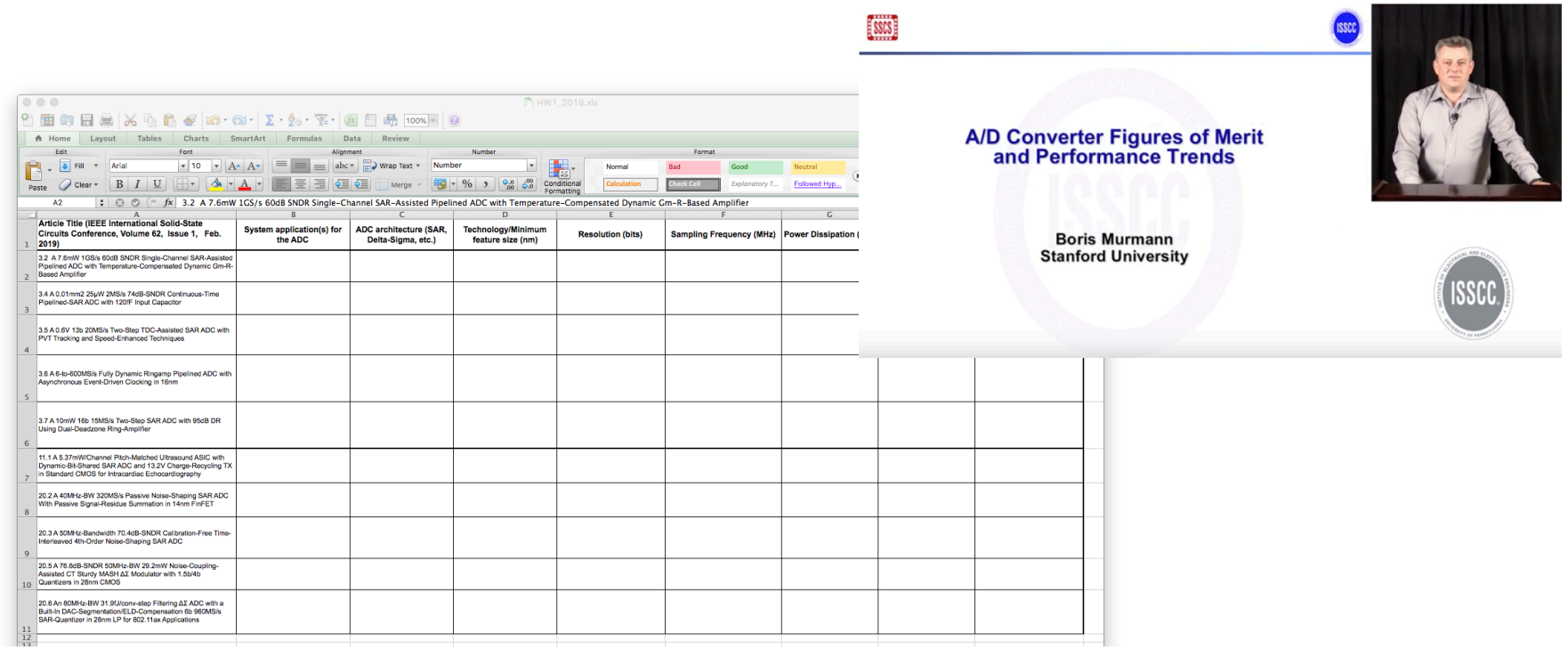
Performance Comparison



B. Murmann, "ADC Performance Survey 1997-2019," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

HW 1

- Read state-of-the-art ADC design publications (2019) and fill out EXCEL spec sheet
- Watch video of ADC performance trends (2014)



Article Title (IEEE International Solid-State Circuits Conference, Volume 62, Issue 1, Feb. 2019)	System application(s) for the ADC	ADC architecture (SAR, Delta-Sigma, etc.)	Technology/Minimum feature size (nm)	Resolution (bits)	Sampling Frequency (MHz)	Power Dissipation
3.2 A 7.8mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier						
3.4 A 0.01mm2 25μW 2MS/s 74dB-SNDR Continuous-Time Pipelined-SAR ADC with 120fF Input Capacitor						
3.5 A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques						
3.6 A 6-to-600MS/s Fully Dynamic Ringamp Pipelined ADC with Asynchronous Event-Driven Clocking in 16nm						
3.7 A 10mW 16b 15MS/s Two-Step SAR ADC with 95dB DR Using Dual-Deadzone Ring-Amplifier						
11.1 A 5.37mW/Channel Pitch-Matched Ultrasound ASIC with Dynamic-Bit-Shared SAR ADC and 13.2V Charge-Recycling TX in Standard CMOS for Intracardiac Echocardiography						
20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC With Passive Signal-Residue Summation in 14nm FinFET						
20.3 A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC						
20.5 A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS						
20.6 An 80MHz-BW 31.9fJ/conv-step Filtering ΔΣ ADC with a Built-In DAC-Segmentation/ELD-Compensation 6b 960MS/s SAR-Quantizer in 28nm LP for 802.11ax Applications						

HW 1

- Read state-of-the-art ADC design publications (2019) and fill out EXCEL spec sheet
- Watch video of ADC performance trends (2014)

- Warning: I don't expect you to understand any of it
- Goal: At the end of the course you will

Course Objective

- Acquire a thorough understanding of the basic principles and challenges in data converter design
  - Focus on concepts that are unlikely to expire within the next decade
  - Preparation for further study of state-of-the-art "fine-tuned" realizations (I.e. Picking the right part for the right problem)
- Strategy
  - Acquire breadth via a complete system walkthrough and a survey of existing architectures
  - Acquire depth through projects that entail design and thorough characterization of a specific circuit example in modern(ish) technology

Admin

- Review Course Websites
  - http://www.seas.upenn.edu/~ese568
  - https://piazza.com/upenn/fall2019/ese568/
  - https://canvas.upenn.edu/courses/
- Complete Diagnostic Quiz!
  - Out now
  - Complete by Friday midnight
- HW 1 out now
  - Look at different performance concerns for ADC