ESE 568: Mixed Signal Circuit Design and Modeling

Lec 11: October 7th, 2019

Sampling Circuits (con't), Switched Capacitor Circuits

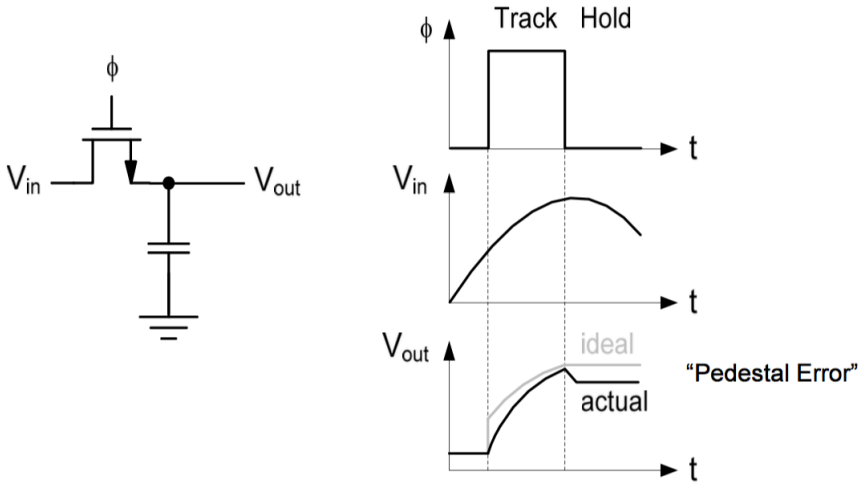
Penn

Lecture Outline

- Elementary track-and-hold
  - Nonidealities (con't)
  - First order improvements
- Advanced techniques
  - Clock bootstrapping (for reference only)
  - Bottom plate sampling
- Switched Capacitor Circuits
  - Charge Redistribution Track-and-hold

Last time...

- Elementary track-and-hold circuit and its non-idealities
- First order improvements to elementary track-and-hold (finish today)

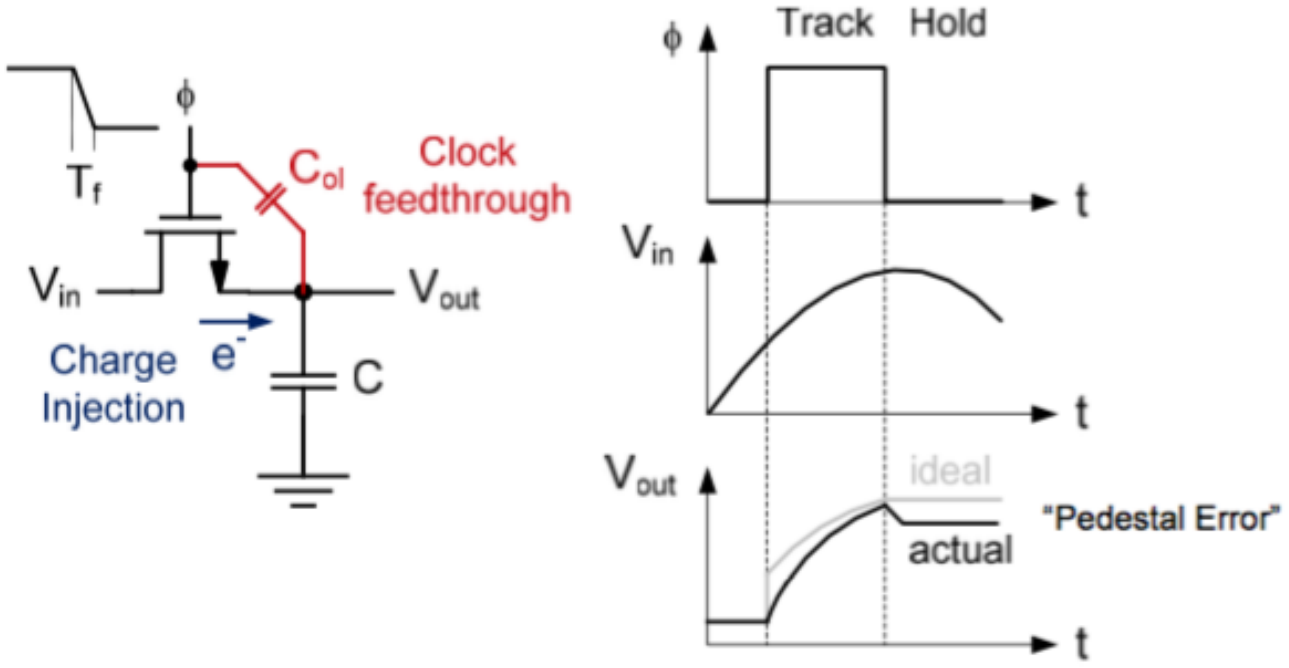


Nonidealities

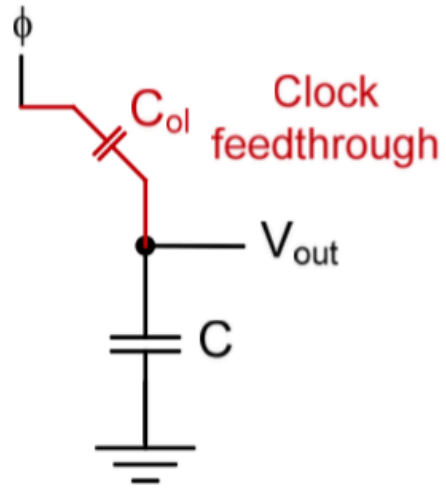
- kTC noise
- Finite acquisition time
- Tracking nonlinearity
- Signal dependent hold instant
- Charge injection and clock feedthrough
- Hold mode feedthrough and leakage
- Clock jitter

Charge Injection and Clock Feedthrough

- Analyze two cases
  - Very Large T_f (slow-gating)
  - Very Small T_f (fast-gating)



Slow Gating Model for $t>t_{off}$



$$V_{out} = V_{in} - \Delta V_{out}$$

$$V_{out} = V_{in} - \frac{C_{ol}}{C_{ol}+C}(V_{in} + V_t - \phi_L) = V_{in}(1+\varepsilon) + V_{os}$$

$$\varepsilon = -\frac{C_{ol}}{C_{ol}+C} \qquad V_{os} = -\frac{C_{ol}}{C_{ol}+C}(V_t - \phi_L)$$

Gain Error Offset Error

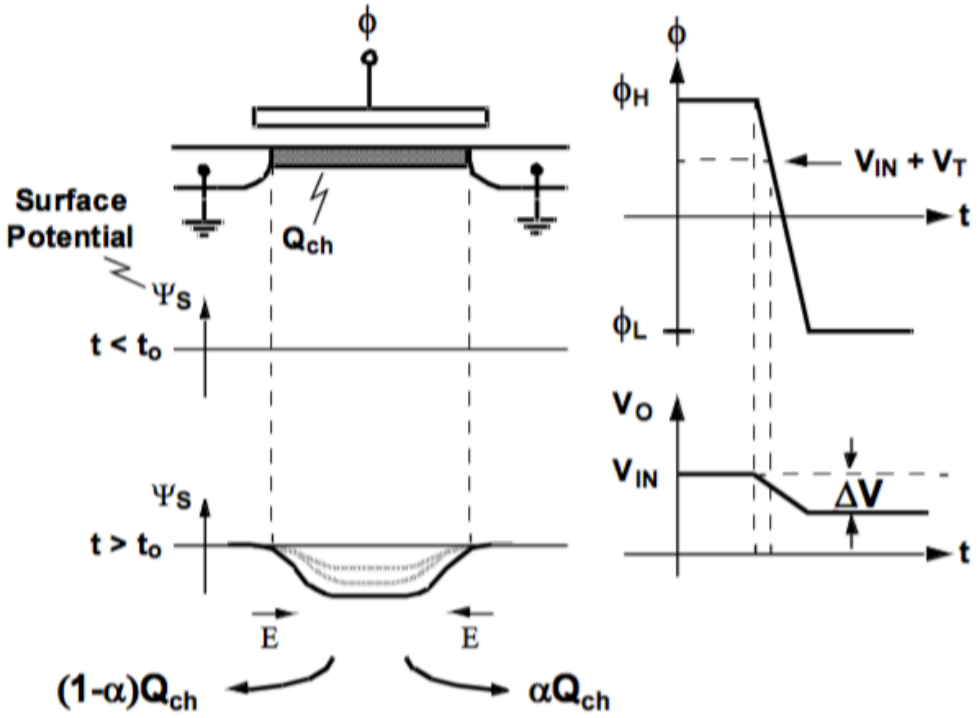
- Example:

$C=1pF,\ \phi_L=0V,\ V_t=0.45V,\ W=20\mu m,\ C_{ol}'=0.1fF/\mu m,\ C_{ol}=2fF$

$\varepsilon = -0.2\%$ $V_{os} = -0.9mV$

Fast Gating

- Channel charge cannot change instantaneously
- Resulting surface potential decays via charge flow to source and drain (charge injection)
- Charge divides between source and drain



Interpretation

- This means that in practice split will have dependence on impedances seen on either side of transistors
- Remember: Slightly more charge will go to side with lower impedance (higher capacitance)

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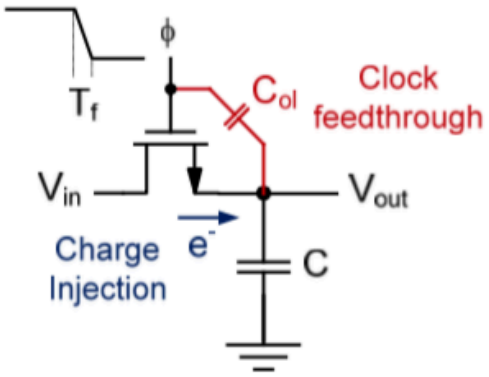

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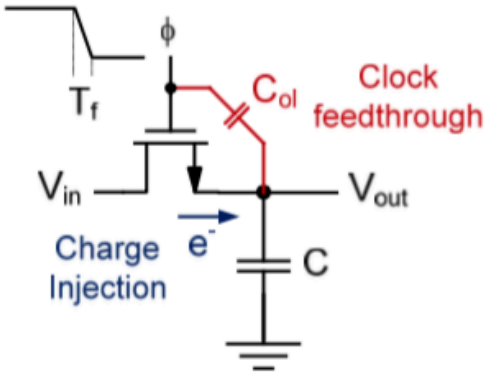

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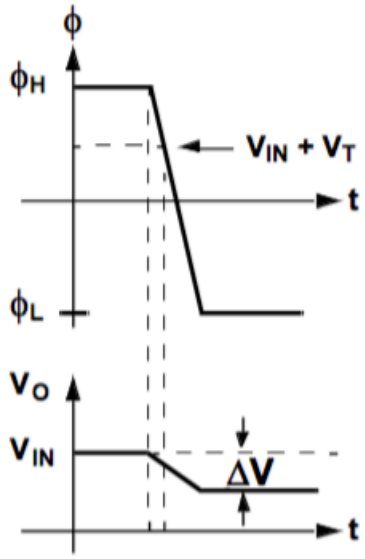
$$V_{out} = V_{in} - \frac{C_{ol}}{C_{ol}+C}(\phi_H - \phi_L) + \frac{1}{2}\frac{Q_{ch}}{C}$$

Assuming 50/50 charge split

$$Q_{ch} = -WLC_{ox}[\phi_H - V_{in} - V_t]$$



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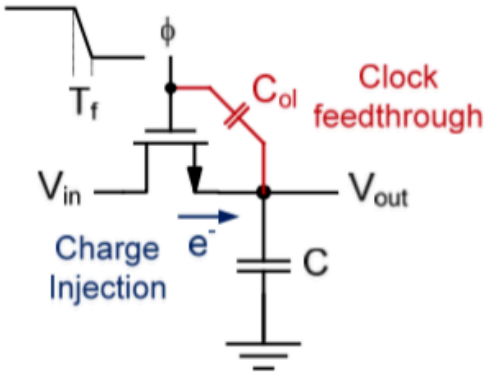

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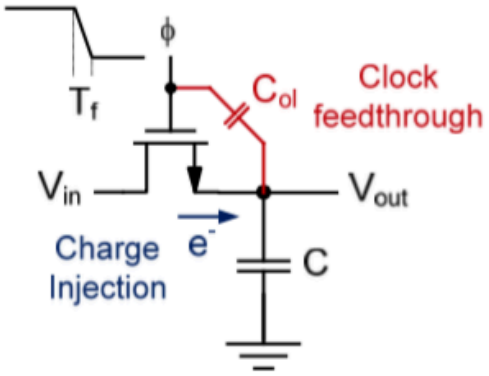

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- Example:

C=1pF, ϕ_H-ϕ_L=1.8V, V_t=0.45V, W=20µm, LC_{ox}=2fF/µm
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$\varepsilon = +2\%$ $\qquad V_{os} = -30.6mV$

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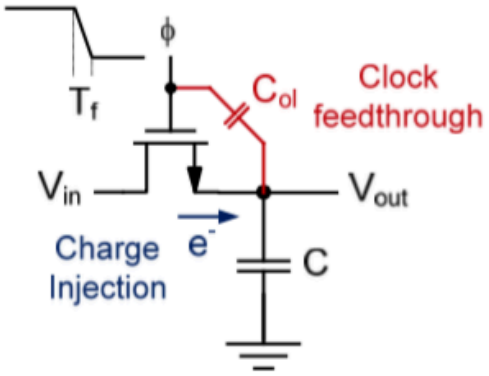

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Assuming 50/50 charge split

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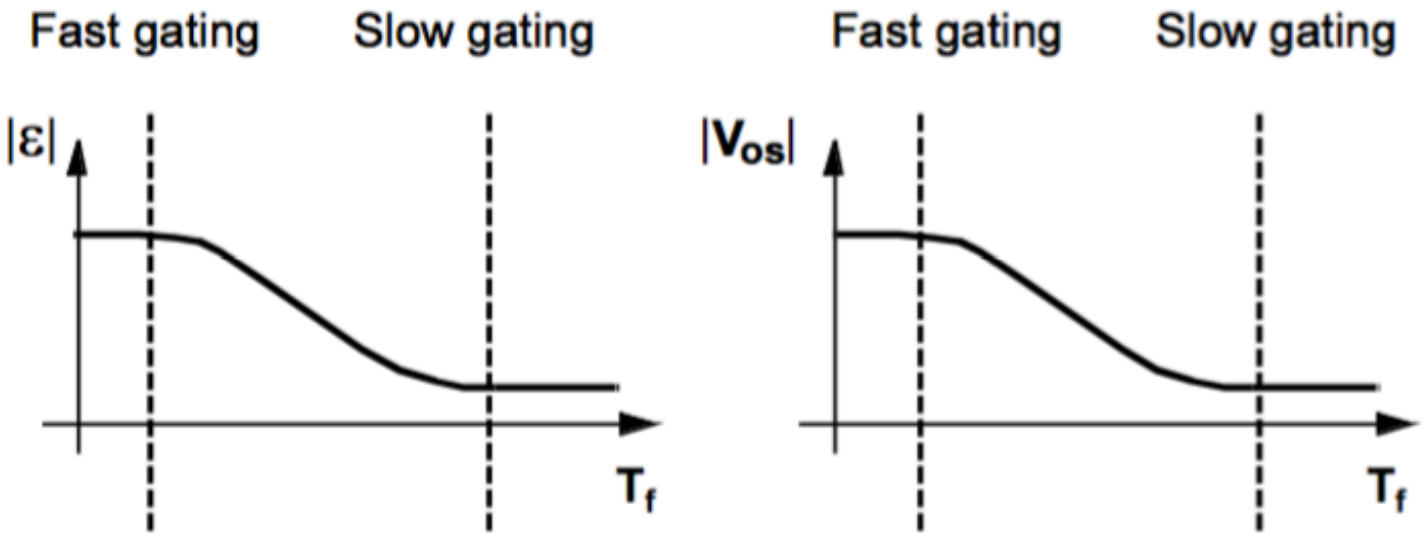
$\varepsilon = +2\%$ $\quad V_{os} = -30.6mV$ Slow gating

$\varepsilon = -0.2\%$ $\quad V_{os} = -0.9mV$

Transition Fast/Slow Gating

- $|\varepsilon|$ and $|V_{OS}|$ decrease as the clock fall time increases and approaches the limit of slow gating
- Practical cases are closer to fast-gating side



Impact of Technology Scaling

- Charge injection error to speed ratio benefits from short channels and increases in mobility

$$\left.\begin{aligned} \Delta V \cong \frac{1}{2}\frac{Q_{ch}}{C} \qquad \frac{1}{2f_s} = \frac{T_s}{2} = N \cdot RC \\ R \cong \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)} \end{aligned}\right\}$$

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$$R \cong \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)} = \frac{L^2}{\mu Q_{ch}}$$

$$\boxed{\frac{\Delta V}{f_s} \cong N\frac{L^2}{\mu}}$$

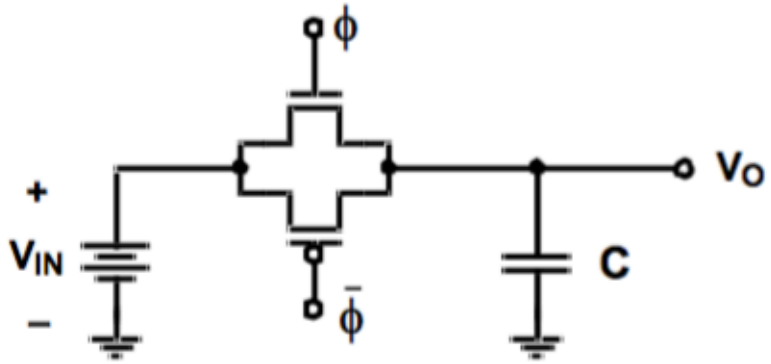
First order improvements

Improvements

- CMOS switch
  - Try to balance nonidealities of nMOS with parallel pMOS
- Charge cancelation
  - Try to cancel charge injection with dummy switch
- Differential Sampling
  - Differential signaling to suppress offset

CMOS Switch Resistance

- In principle, adding PMOS helps with signal dependent R_{on} in track mode
  - Parallel resistance of MOS devices roughly constant



$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{GSn} - V_{tn})} \Bigg\| \frac{1}{\mu_p C_{ox}\left[\frac{W}{L}\right]_p \left(|V_{GSp}| - |V_{tp}|\right)}$$

Analysis

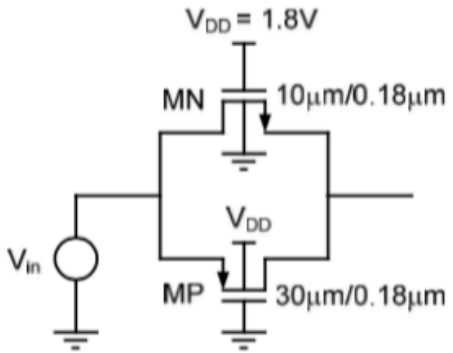
$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{GSn} - V_{tn})} \Bigg\| \frac{1}{\mu_p C_{ox}\left[\frac{W}{L}\right]_p (|V_{GSp}| - |V_{tp}|)}$$

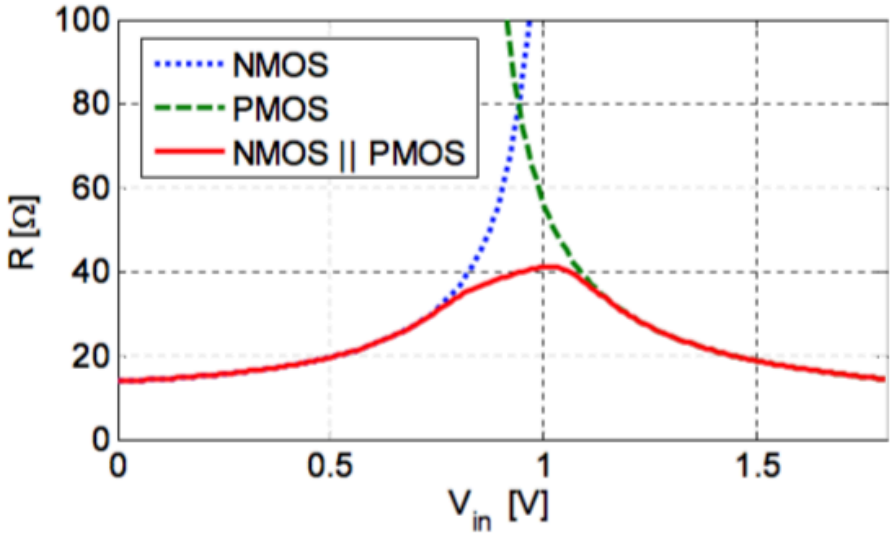
$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{DD} - V_{tn}) - \left(\mu_n C_{ox}\left[\frac{W}{L}\right]_n - \mu_p C_{ox}\left[\frac{W}{L}\right]_p\right) v_{in} - \mu_p C_{ox}\left[\frac{W}{L}\right]_p |V_{tp}|}$$

$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{DD} - V_{tn} - |V_{tp}|)} \quad \text{if} \quad \mu_n\left[\frac{W}{L}\right]_n = \mu_p\left[\frac{W}{L}\right]_p$$

- Independent of V_{in} → too good to be true!
- Missing factors
  - Backgate effect
  - Short channel effects

Real CMOS Switch

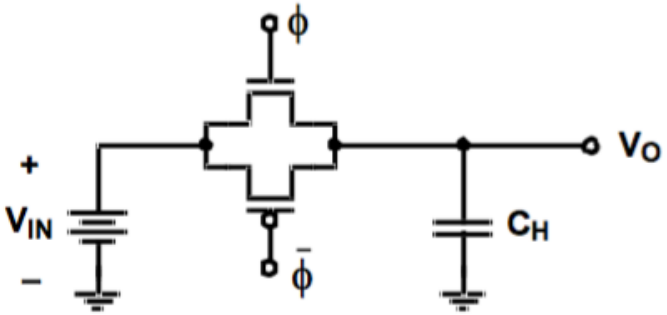




- Design
  - Size P/N ratio to minimize change in R over input range
- PMOS bring limited benefit unless the input signal range is large or centered near V_{DD}

Charge Cancellation: CMOS Switch

- Partial cancellation of offset error
- Assuming fast gating, 50/50 charge split and $W_nL_n=W_pL_p$



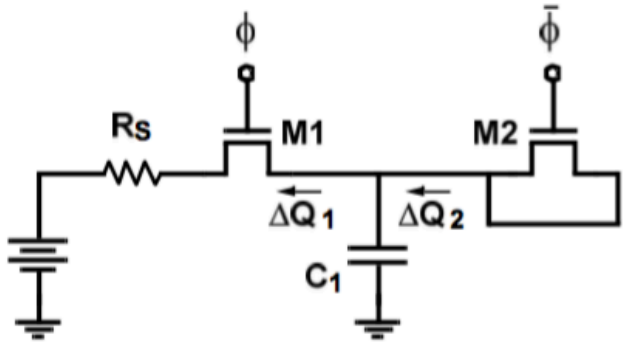
$$Q_{chn} \cong -W_nL_nC_{ox}\left(\phi_H - V_{IN} - V_{tn}\right)$$

$$Q_{chp} \cong W_pL_pC_{ox}\left(V_{IN} - \phi_L - \left|V_{tp}\right|\right)$$

$$\Delta V_o \cong \frac{\frac{1}{2}Q_{chn} + \frac{1}{2}Q_{chp}}{C} = \frac{C_{ox}}{C}\left(V_{IN} - \frac{\phi_H - \phi_L}{2} + \frac{V_{tn} - \left|V_{tp}\right|}{2}\right)$$

- Charges full cancel for $V_{in}=(V_H-V_L)/2=V_{DD}/2$ and $V_{tn}=-V_{tp}$
  - Still signal dependent residual injection

Charge Cancellation: Dummy Switch



$$\Delta Q_1 = 0.5Q_{ch1} + Q_{ol1}$$

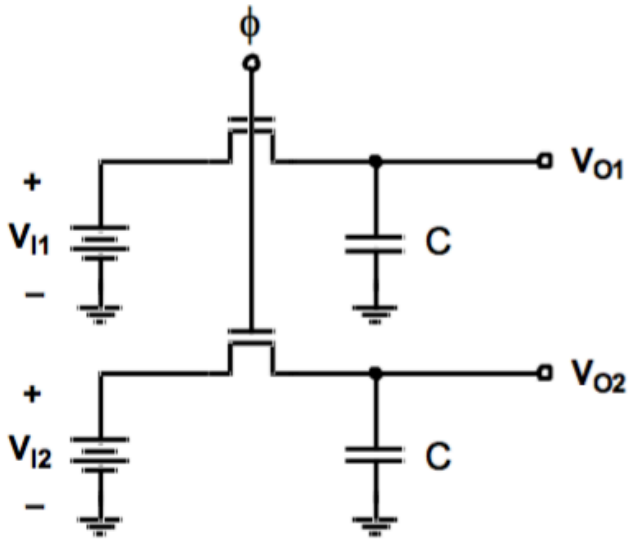
$$\Delta Q_2 \cong Q_{ch2} + 2Q_{ol2} \cong 0.5Q_{ch1} + Q_{ol1}$$

$$\Delta Q_1 - \Delta Q_2 \cong 0$$

[Eichenberger and Guggenbűhl, JSSC 8/89]

- Cancellation is never perfect, since channel charge of M1 will not be 50/50 split
  - If R_s small, most of charge will flow toward the input voltage source
  - ~80% cancellation
- Not precision technique, just a partial clean-up attempt

Differential Sampling



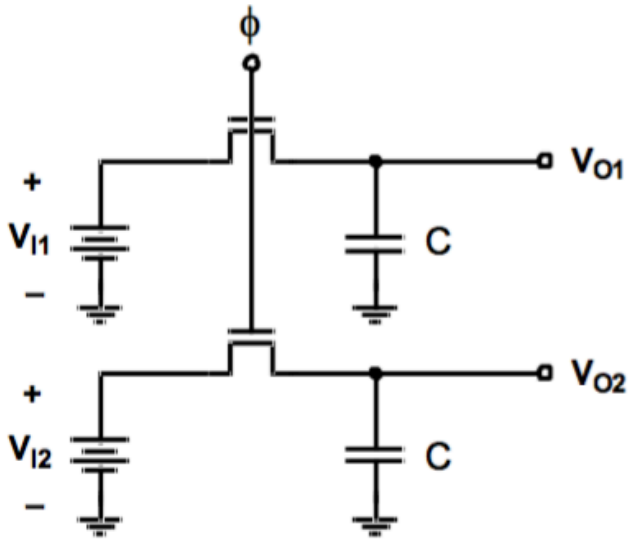
$$V_{ID} = V_{I1} - V_{I2} \qquad V_{OD} = V_{O1} - V_{O2}$$

$$V_{IC} = \frac{V_{I1} + V_{I2}}{2} \qquad V_{OC} = \frac{V_{O1} + V_{O2}}{2}$$

$$V_{O1} = (1+\varepsilon_1)V_{I1} + V_{OS1}$$

$$V_{O2} = (1+\varepsilon_2)V_{I2} + V_{OS2}$$

Differential Sampling



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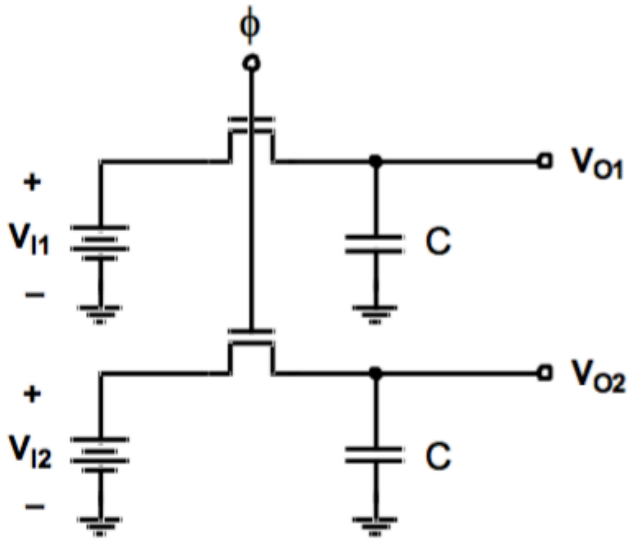
$$V_{O1} = (1+\varepsilon_1)V_{I1} + V_{OS1}$$

$$V_{O2} = (1+\varepsilon_2)V_{I2} + V_{OS2}$$

$$V_{OD} = \left(1+\frac{\varepsilon_1+\varepsilon_2}{2}\right)V_{ID} + (\varepsilon_1-\varepsilon_2)V_{IC} + (V_{OS1}-V_{OS2}) \cong \left(1+\frac{\varepsilon_1+\varepsilon_2}{2}\right)V_{ID}$$

Differential Sampling



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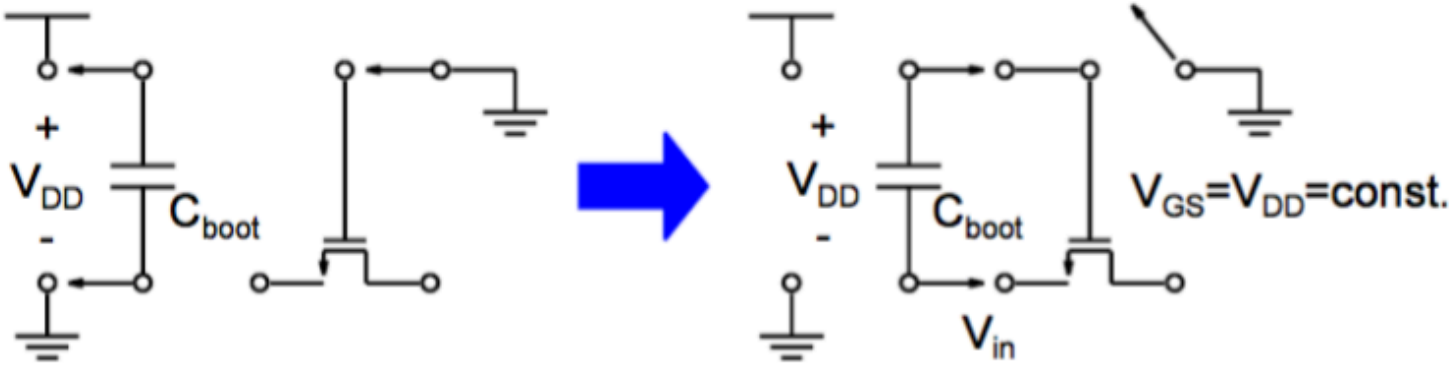
$$V_{OC} = \left(\frac{\varepsilon_1-\varepsilon_2}{4}\right)V_{ID} + \left(1+\frac{\varepsilon_1+\varepsilon_2}{2}\right)V_{IC} + \left(\frac{V_{OS1}+V_{OS2}}{2}\right) \cong \left(1+\frac{\varepsilon_1+\varepsilon_2}{2}\right)V_{IC} + \left(\frac{V_{OS1}+V_{OS2}}{2}\right)$$

Differential Sampling

- Assuming good matching between the two half circuits, we have all benefits of differential signaling
  - Small residual offset in V_{OD}
  - Good rejection of coupling noise, supply noise, …
  - Small common-mode to differential-mode gain
- Unfortunately, V_{OD} has same gain error as basic single-ended circuit
- Also have nonlinear terms
  - Simplistic models assume channel charge linearly related to V_{in} (ignoring higher order effects, e.g. backgate effect)
    - Expect to see nonlinear distortion along with gain error

Advanced Techniques

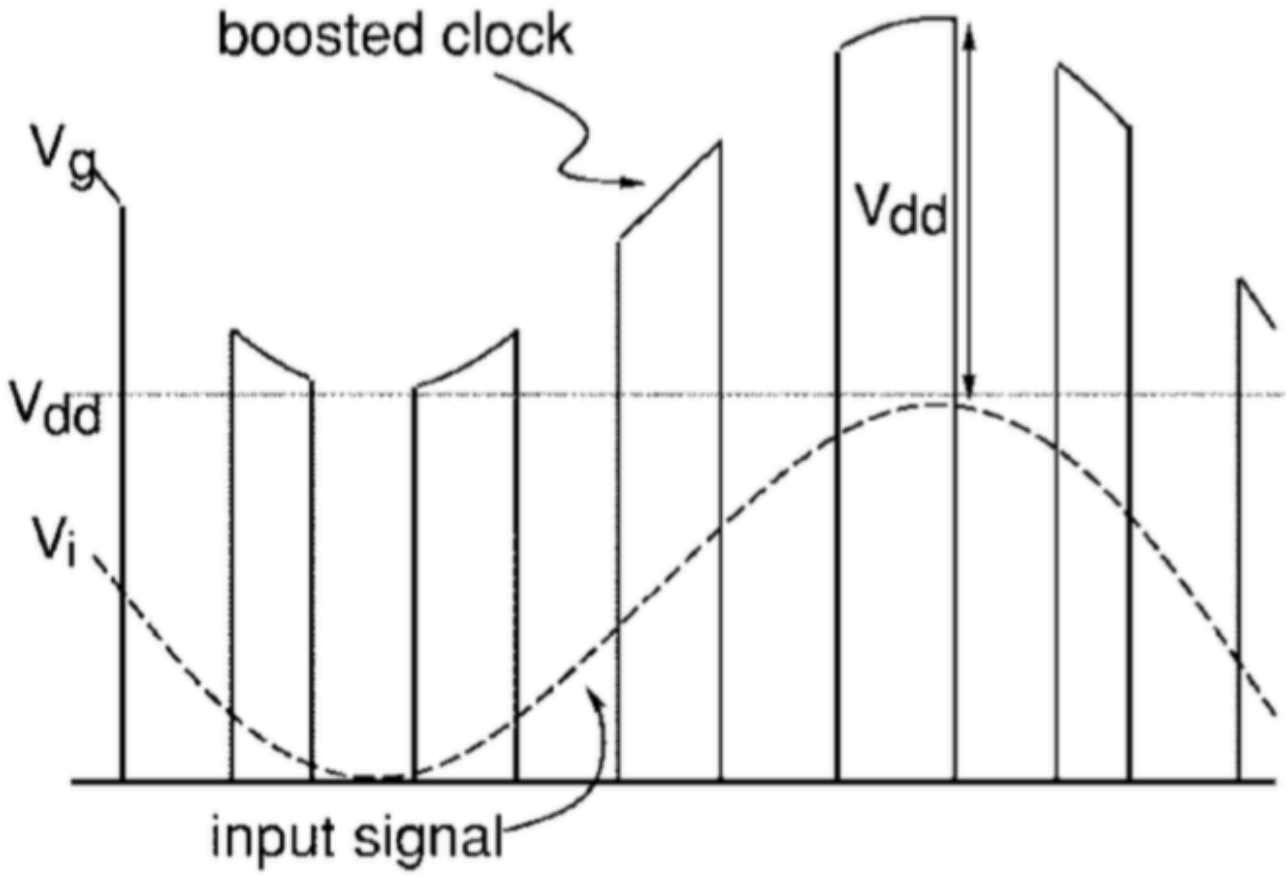
Clock Bootstrapping (Reference)



A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," PhD Thesis, UC Berkeley, 1999.

- Phase 1
  - C_{boot} is precharged to V_{DD}
  - Sampling switch is off
- Phase 2
  - Sampling switch is on with $V_{GS}=V_{DD}$=const.
  - To first order, both R_{ON} and channel charge are signal independent

Waveforms (Reference)



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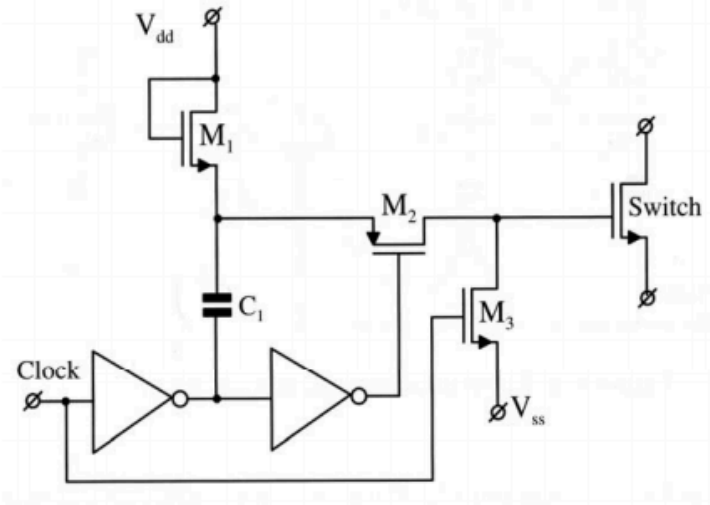
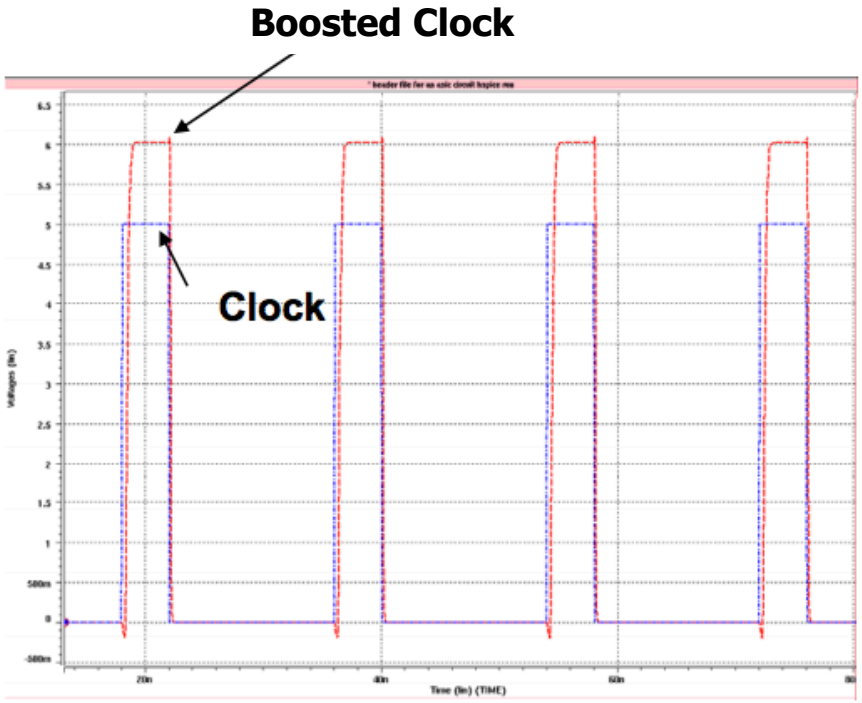
Basic Clock Bootstrap Circuit (Reference)

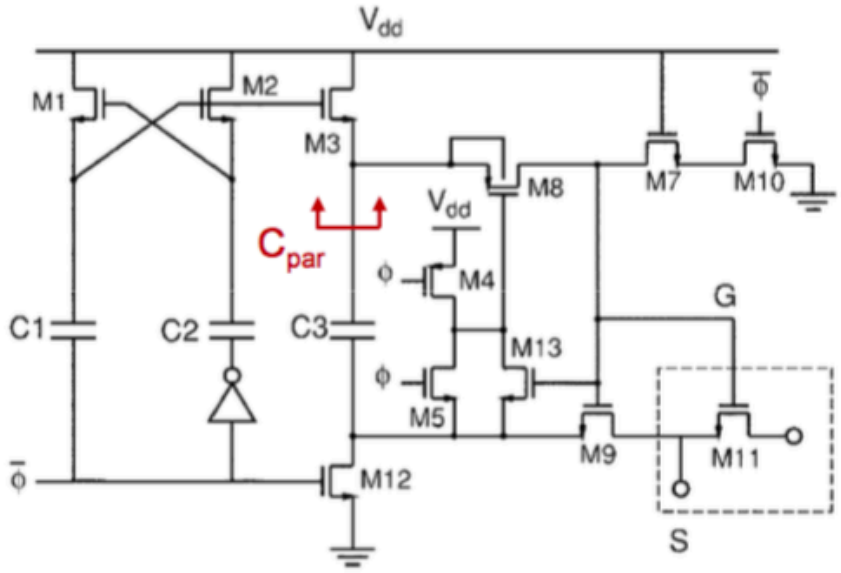




Simulation Result

Circuit Implementation (Reference)

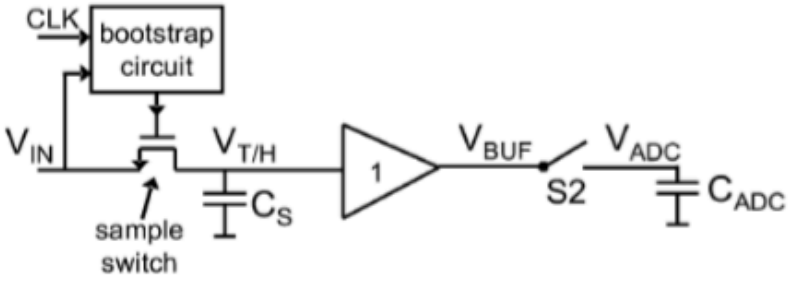
- Efficacy of bootstrap circuit is reduced by
  - Backgate effect
  - Parasitic Capacitance between at top plate of C3



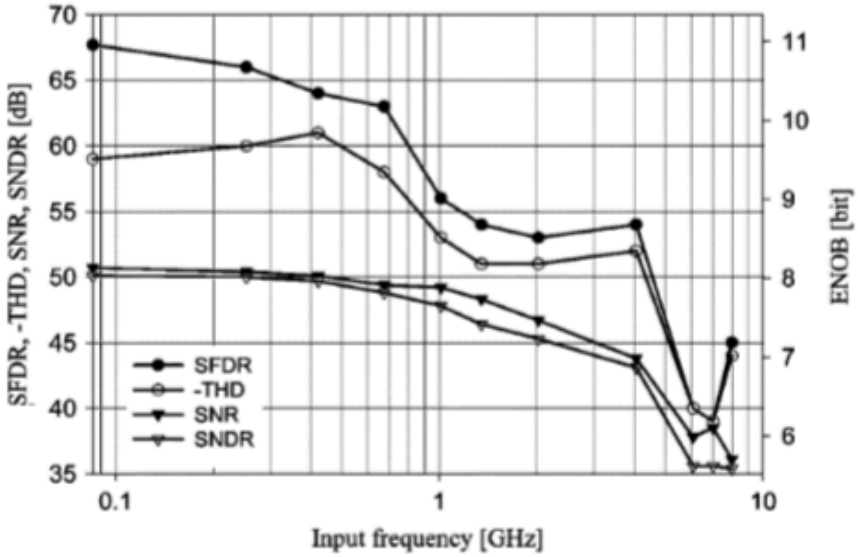
$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n\left(\frac{C_{boot}}{C_{boot}+C_{par}}V_{DD}-\frac{C_{par}}{C_{boot}+C_{par}}V_{in}-\underbrace{V_{tn}[V_{in}]}_{\text{Backgate effect}}\right)}$$

Performance of Bootstrapped Samplers (Reference)

- Bootstrapped sampling tends to work well up to ~10bit resolution



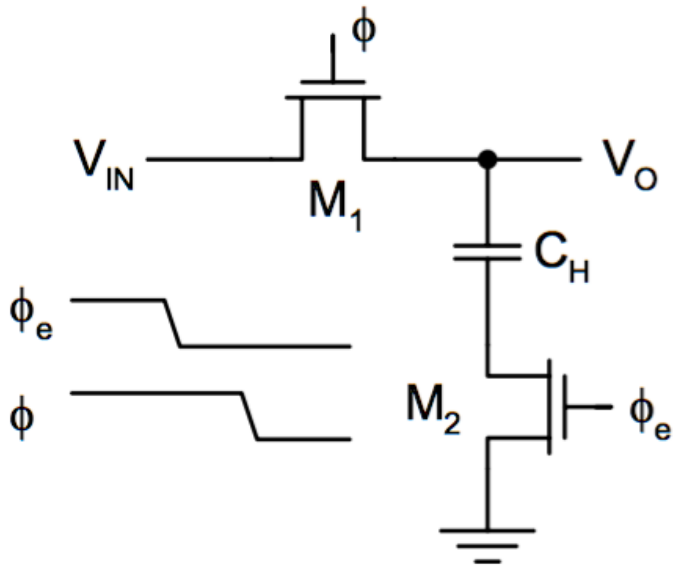
[Louwsma, JSSC 4/2008]



Bottom Plate Sampling

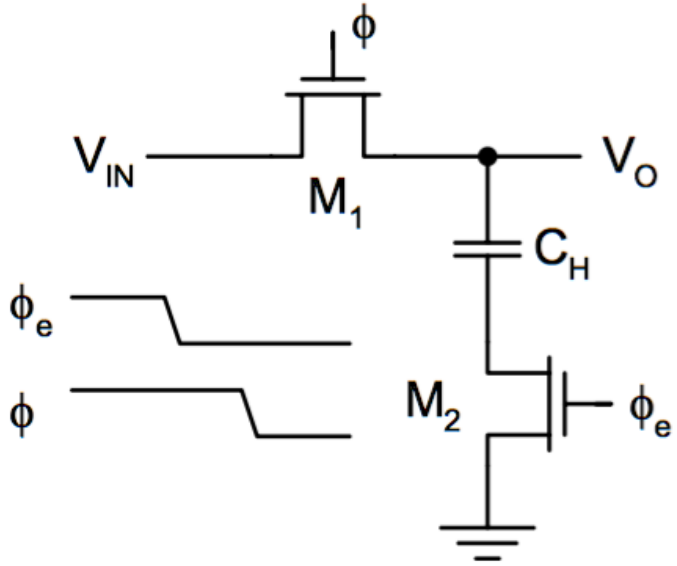
- What if we want to do much better, e.g. 16 bits?
- Basic idea
  - Sample signal at the "grounded" side of the capacitor to achieve signal independence
- References
  - D. J. Allstot and W. C. Black, Jr., "Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," Proc. IEEE, pp. 967-986, Aug. 1983.
  - K.-L. Lee and R. G. Meyer, "Low-Distortion Switched- Capacitor Filter Design Techniques," IEEE J. Solid-State Circuits, pp. 1103-1113, Dec. 1985.
- First look at single ended circuit

Bottom Plate Sampling Analysis



Bottom Plate Sampling Analysis

- Turn M2 off "slightly" before M1
- Typically a few hundred ps delay between falling edges of ϕ_e and ϕ



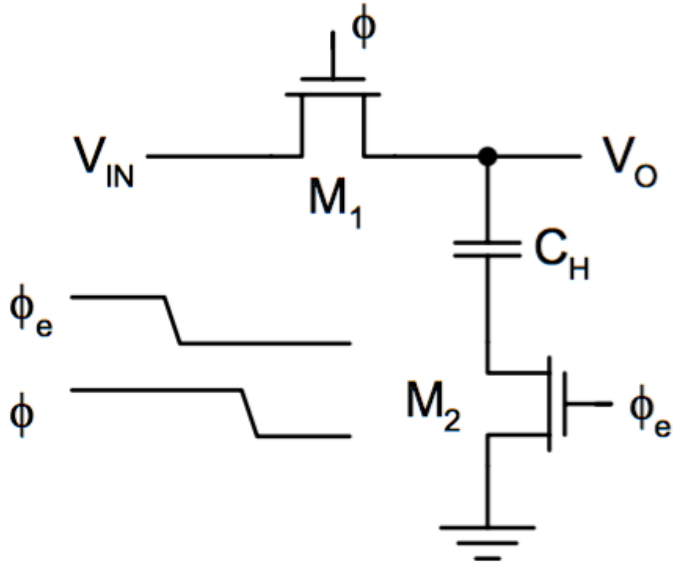
Bottom Plate Sampling Analysis

- Turn M2 off "slightly" before M1
- Typically a few hundred ps delay between falling edges of ϕ_e and ϕ
- During turn off, M2 injects charge

$$\Delta Q_2 \cong \alpha_2 W L C_{ox}(\phi_H - V_{tn})$$

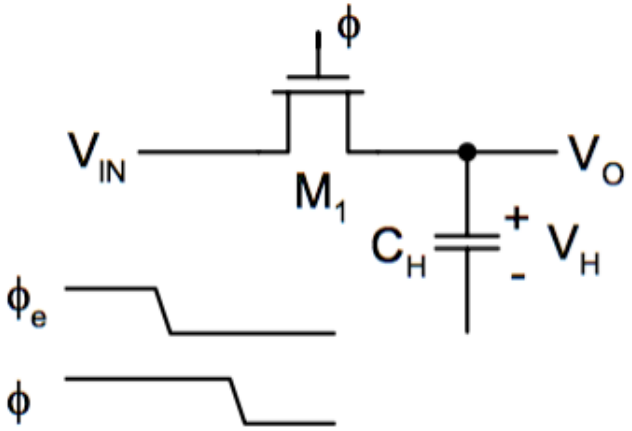
- To first order, charge injected by M2 is signal independent!
- Voltage across C_H

$$V_H = V_{IN} - \frac{\Delta Q_2}{C_H}$$



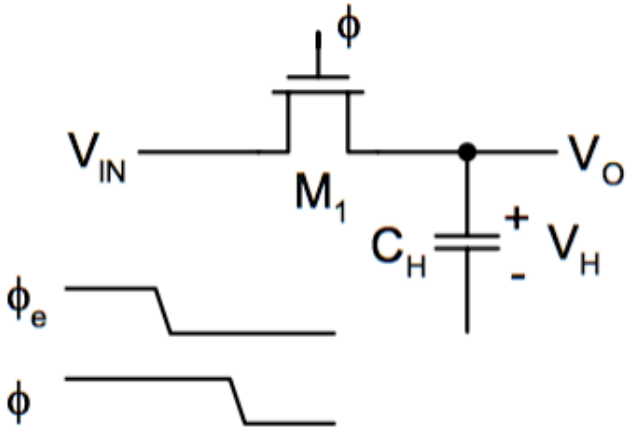
Bottom Plate Sampling Analysis

- Next, turn off M_1
- Since bottom plate of C_H is floating, there is no way to change its stored charge
  - M1 cannot inject any charge onto C_H
  - Most of M_1's charge injection goes to input source and/or onto parasitics at node V_O



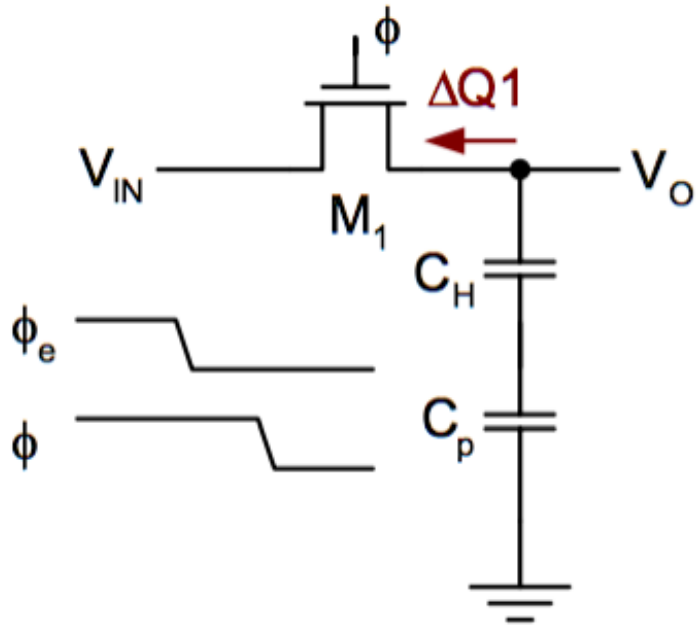
Bottom Plate Sampling Analysis

- Next, turn off M_1
- Since bottom plate of C_H is floating, there is no way to change its stored charge
  - M1 cannot inject any charge onto C_H
  - Most of M_1's charge injection goes to input source and/or onto parasitics at node V_O
- But, is the bottom plate really floating?



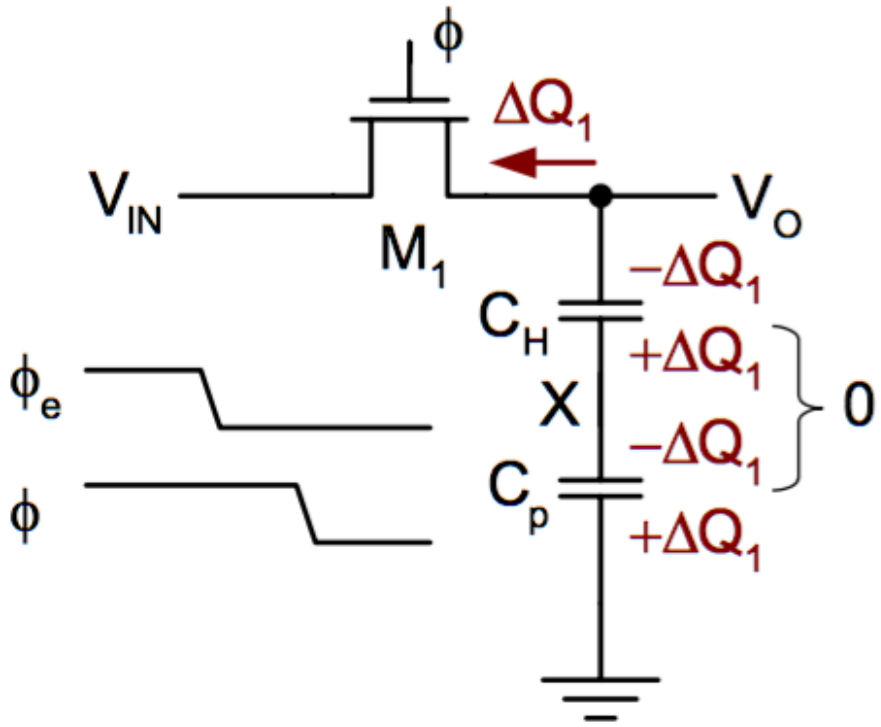
Bottom Plate Sampling Analysis

- Bottom plate not really floating…
  - There must be some parasitic cap, e.g. M2 drain-to-bulk capacitance
- So, in real life, M1 does inject charge onto C_H
  - How much?



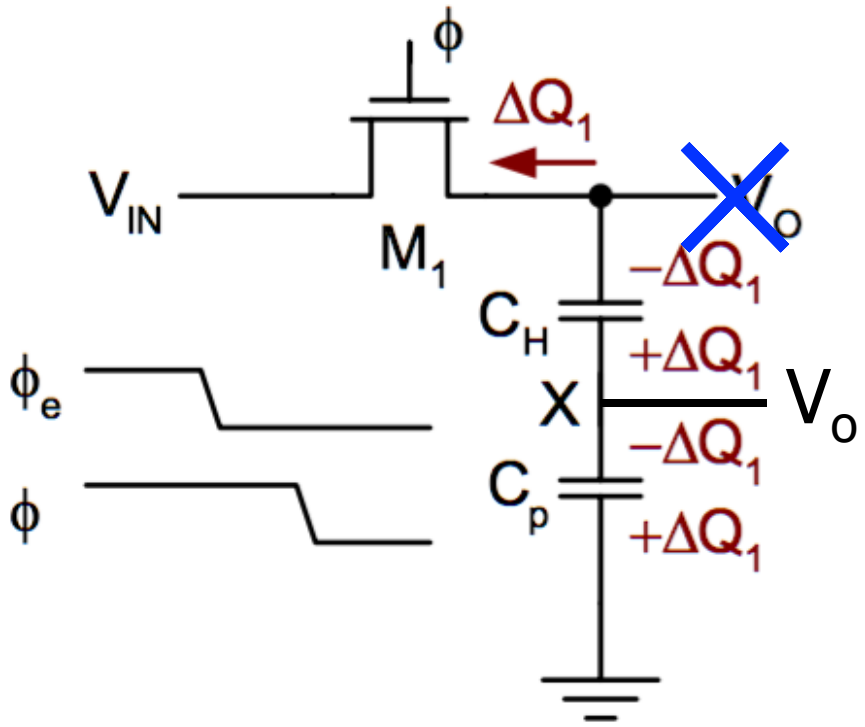
Bottom Plate Sampling Analysis

- Interesting observation
  - Even if M1 injects some charge onto C_H, the total charge at node X cannot change!



Bottom Plate Sampling Analysis

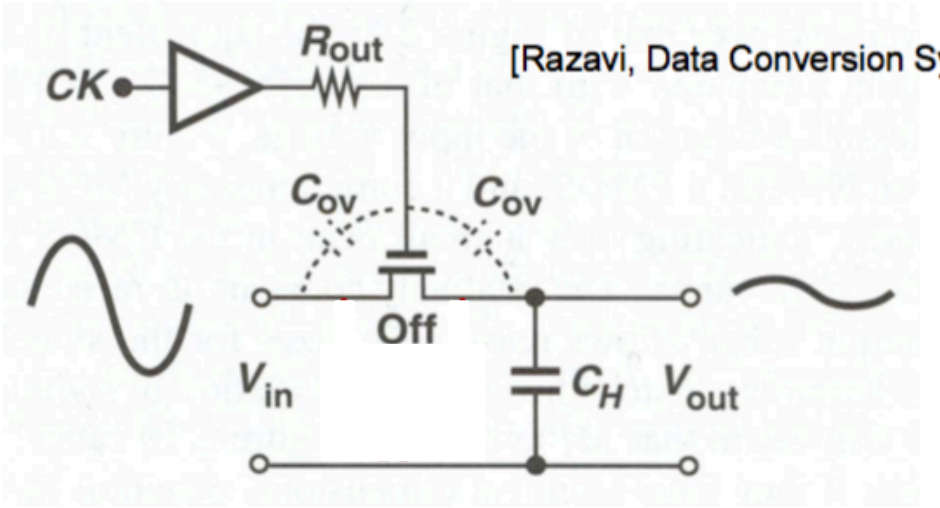
- Interesting observation
  - Even if M1 injects some charge onto C_H, the total charge at node X cannot change!
- Idea
  - Process total charge at node X instead of looking at voltage across C_H



Nonidealities

- kTC noise
- Finite acquisition time
- Tracking nonlinearity
- Signal dependent hold instant
- Charge injection and clock feedthrough
- Hold mode feedthrough and leakage
- Clock jitter

Hold Mode Feedthrough

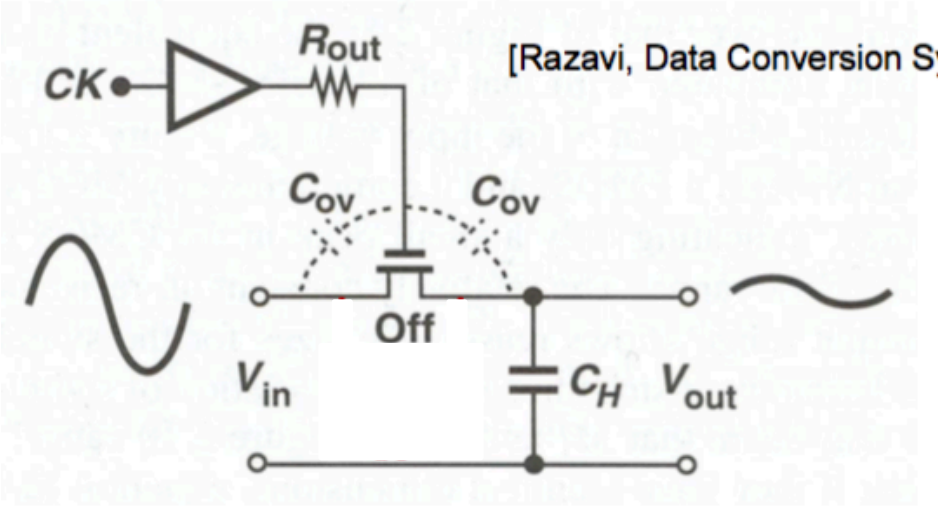


[Razavi, Data Conversion System Design, p.17]

$$\left.\frac{V_{out}}{V_{in}}\right|_{hold} \approx \frac{C_{ov}}{C_H}\frac{R_{out}C_{ov}s}{2R_{out}C_{ov}s+1}$$

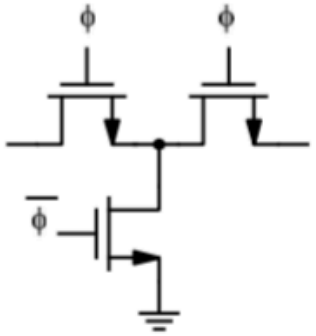
- Want to make R_{out} as small as possible

Hold Mode Feedthrough

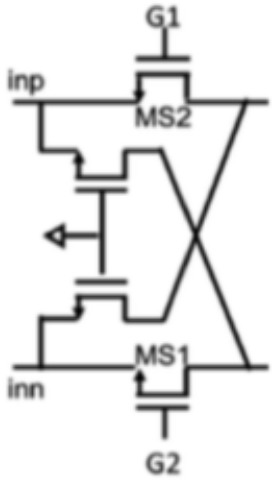


[Razavi, Data Conversion System Design, p.17]

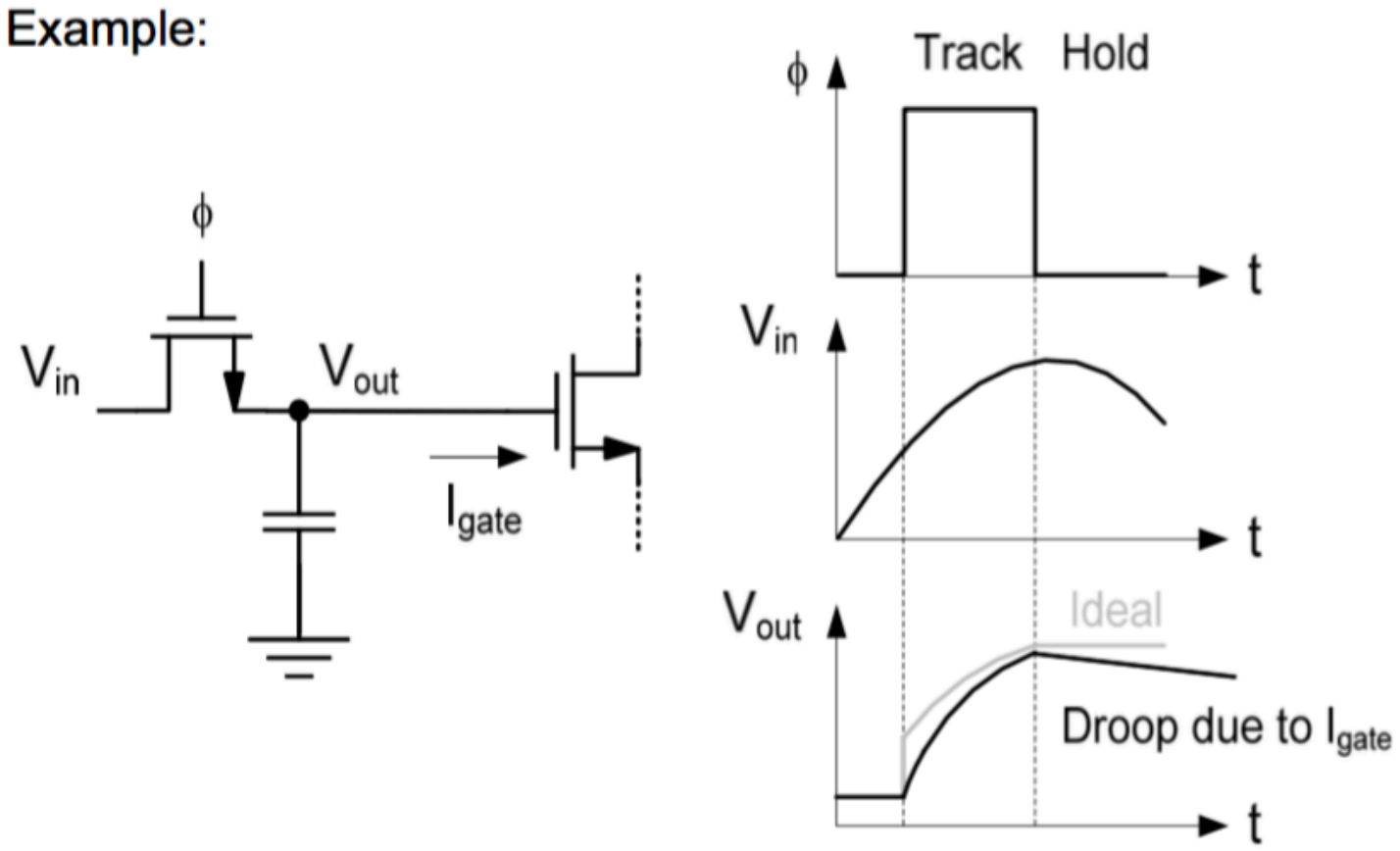
T-switch



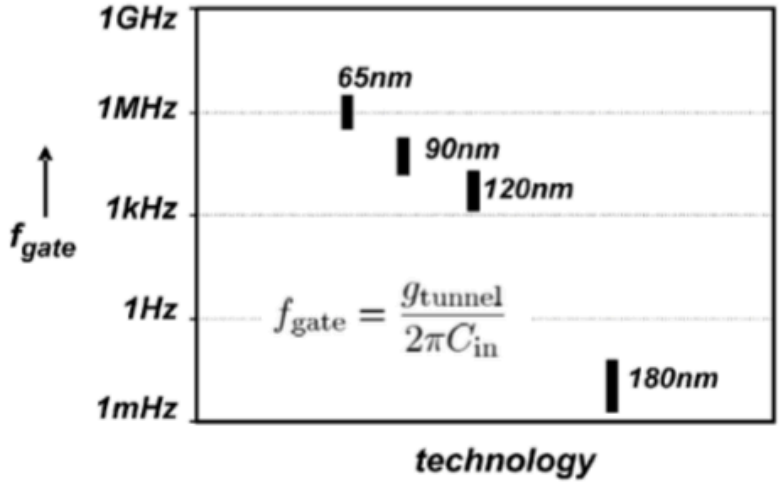
- T-Switch for low speed applications
- Cross coupling for high speed applications



Hold Mode Leakage



Gate Leakage Data



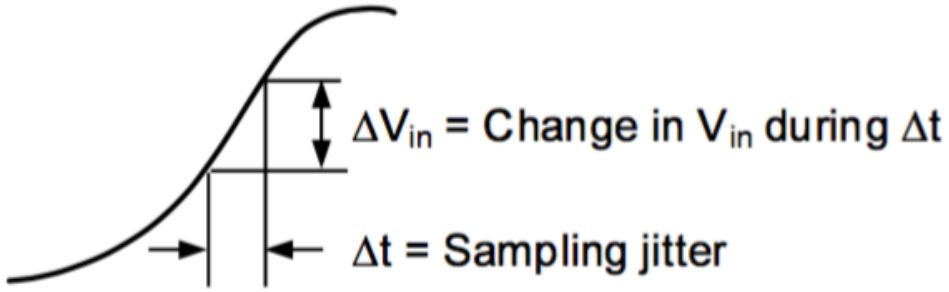
A. Annema, et al., "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits*, pp. 132-143, Jan. 2005.

$$\frac{dv_C}{dt} \approx -\gamma_{dv\,dt} \cdot f_{\text{gate}} \left[\frac{V}{s}\right] \quad \text{with } \gamma_{dv\,dt} \approx 1\text{ V}.$$

- In 65nm CMOS, gate capacitance droop rate is 1V/ μ s!
- Later process use high-k dielectrics

Sampling Jitter

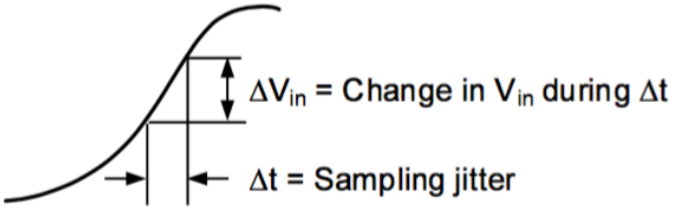
- In any sampling circuit, electronic noise causes random timing variations in the actual sampling clock edge
  - Adds "noise" to samples, especially if dV_{in}/dt is large



$$\Delta V_{in} \cong \frac{dV_{in}}{dt} \cdot \Delta t$$

- Analysis
  - Consider sine wave input signal
  - Assume Δt is random with zero mean and standard deviation σ_t

Analysis



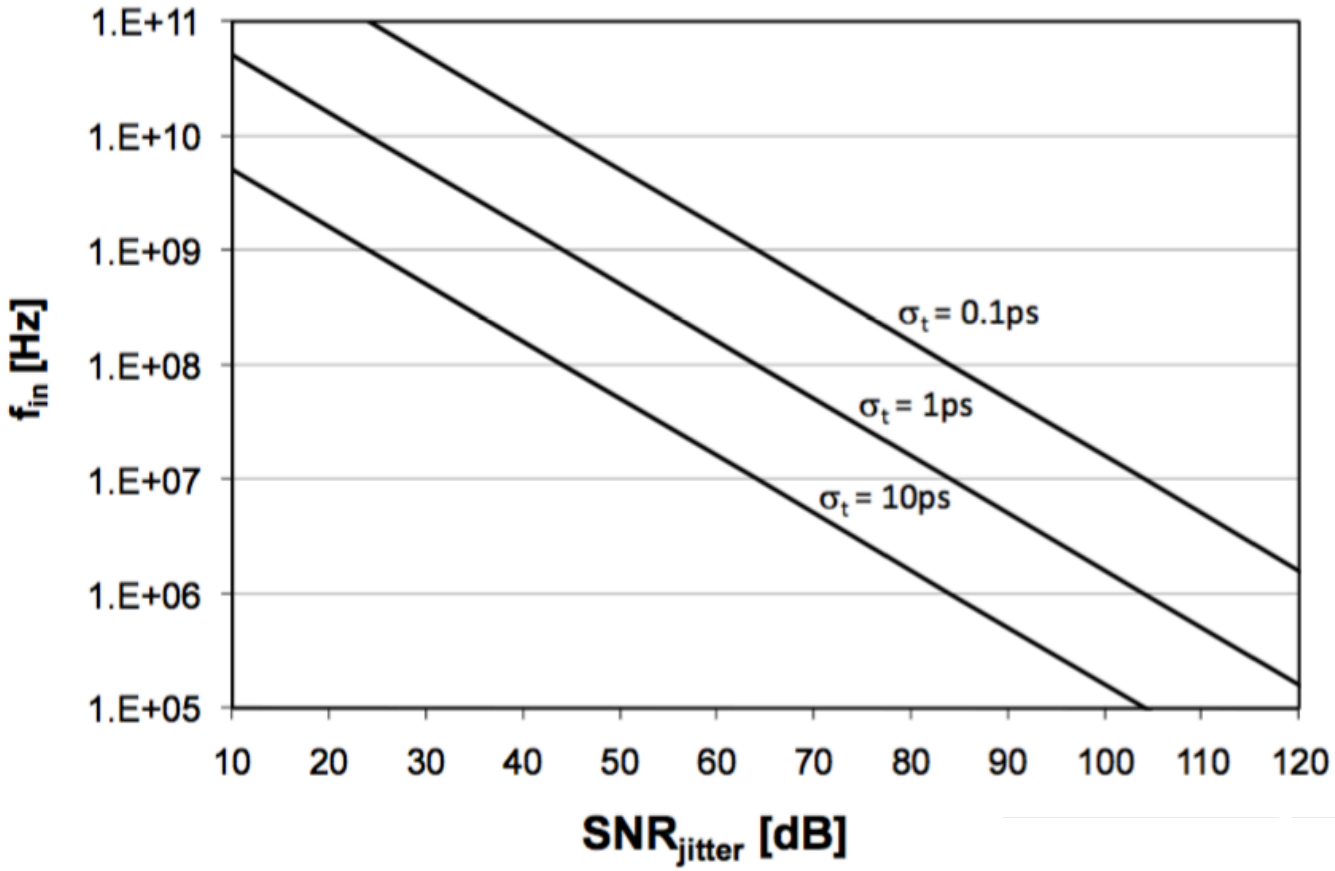
$$\Delta V_{in} \cong \frac{dV_{in}}{dt} \cdot \Delta t$$

$$E\left\{\Delta V_{in}^2\right\} \cong E\left\{\left(\frac{dV_{in}}{dt}\right)^2 \cdot \Delta t^2\right\} = E\left\{\left(\frac{dV_{in}}{dt}\right)^2\right\} \cdot E\left\{\Delta t^2\right\}$$

$$\cong E\left\{\left(\frac{d}{dt} A\cos\left[2\pi \cdot f_{in} \cdot t\right]\right)^2\right\} \cdot \sigma_t^2 \cong \frac{1}{2}\left(2\pi \cdot A \cdot f_{in}\right)^2 \cdot \sigma_t^2$$

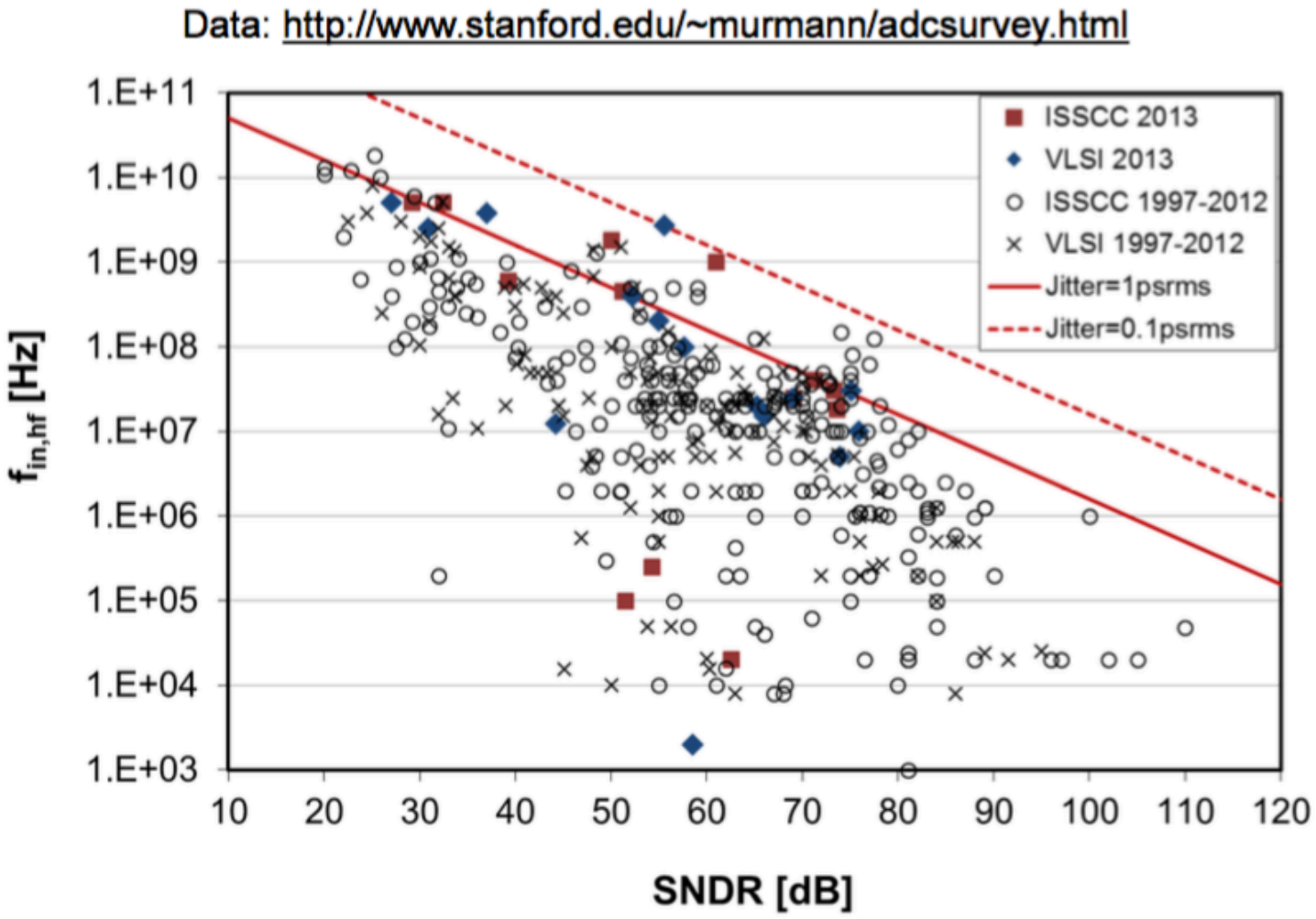
$$SNR_{jitter} = \frac{\frac{1}{2}A^2}{\frac{1}{2}A^2\omega_{sin}^2 \cdot \sigma_t^2} = \frac{1}{\omega_{sin}^2 \cdot \sigma_t^2}$$

Result



$$SNR_{jitter} = \frac{1}{\omega_{sin}^2 \cdot \sigma_t^2}$$

ADC Performance Survey (ISSCC & VLSI)



Significance of Jitter

- In light of the above, sampling jitter has become one of the main showstoppers for further improvements in the ADC speed-resolution product

$$SNR_{jitter} = \frac{\frac{1}{2}A^2}{\frac{1}{2}A^2\omega_{sin}^2 \cdot \sigma_t^2} = \frac{1}{\omega_{sin}^2 \cdot \sigma_t^2}$$

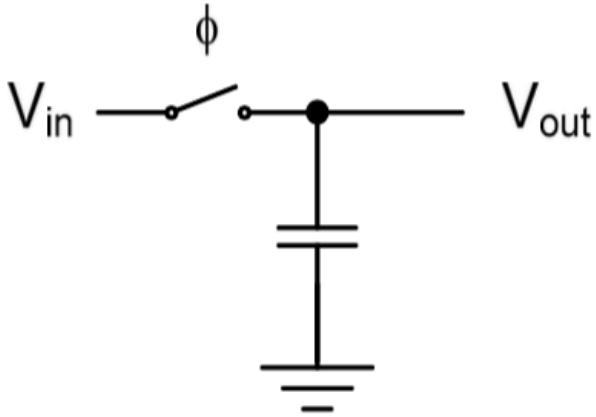
- Example
  - F_{in}=10MHz, σ_t=300ps → SNR_{jitter} = 34.5dB
- Not great, but in many applications, the signal is not a sinusoid, but spread in some way across frequency
- Proper analysis must take into account signal properties
  - See Da Dalt, TCAS1, 9/2002
  - Autocorrelation analysis

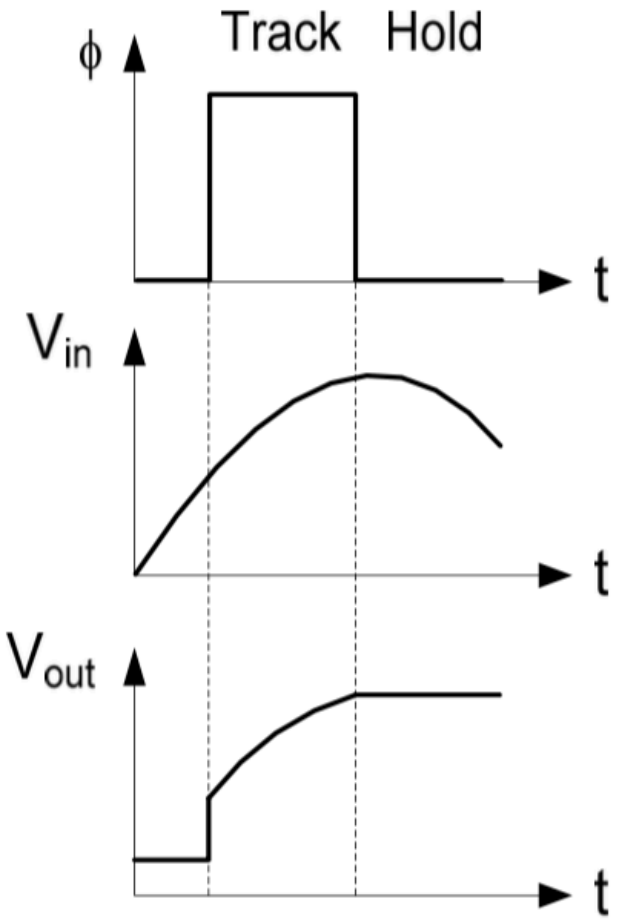
Switched Capacitor Circuits

Interesting Switched Capacitor Circuits

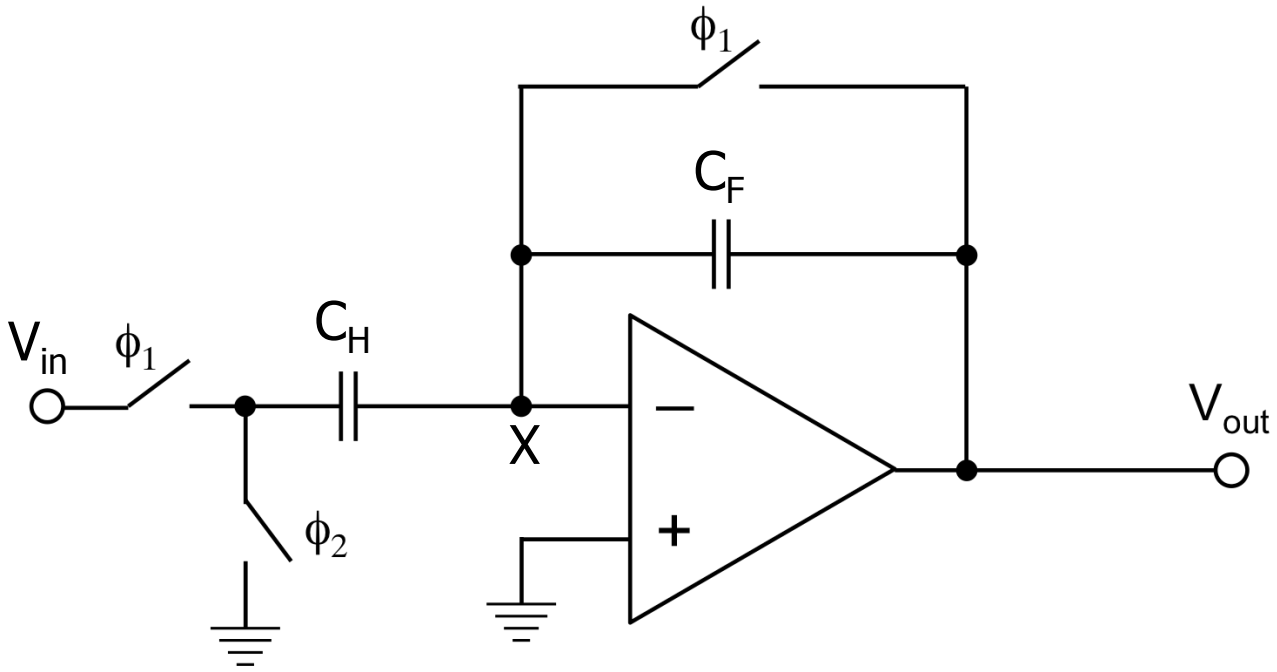
- Track & Hold
  - Charge redistribution T/H with common mode cancellation
  - Flip-around T/H
- SC Difference amplifiers
  - Used e.g. in pipeline ADCs
- SC Integrators
  - Used e.g. in sigma-delta ADCs
- Passive charge redistribution networks
  - Used e.g. in successive approximation ADCs

Ideal Track-and-Hold Circuit



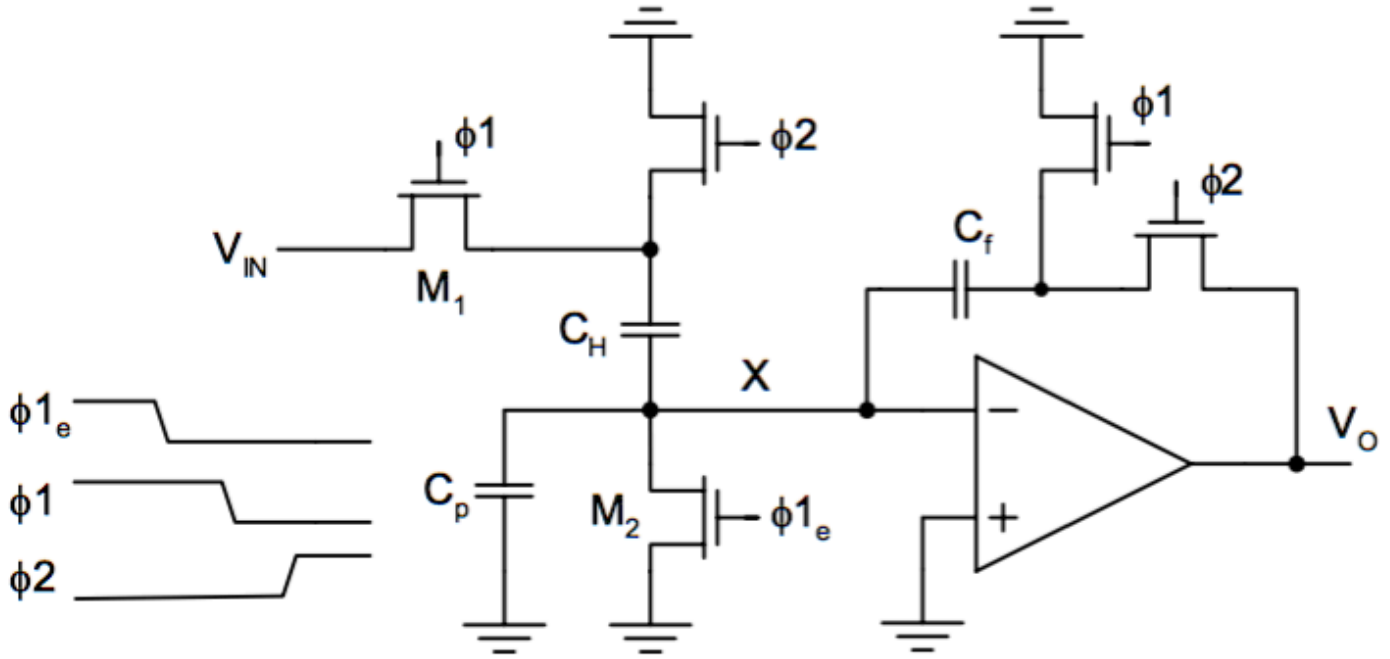


Charge Redistribution Track&Hold

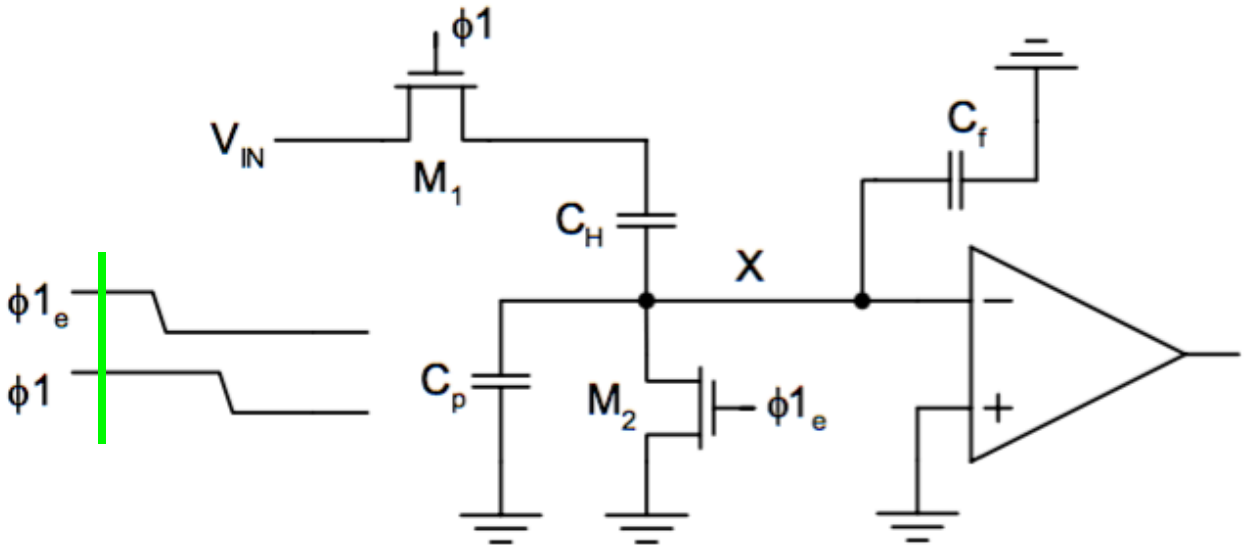


Charge Redistribution Track&Hold

- With bottom plate sampling

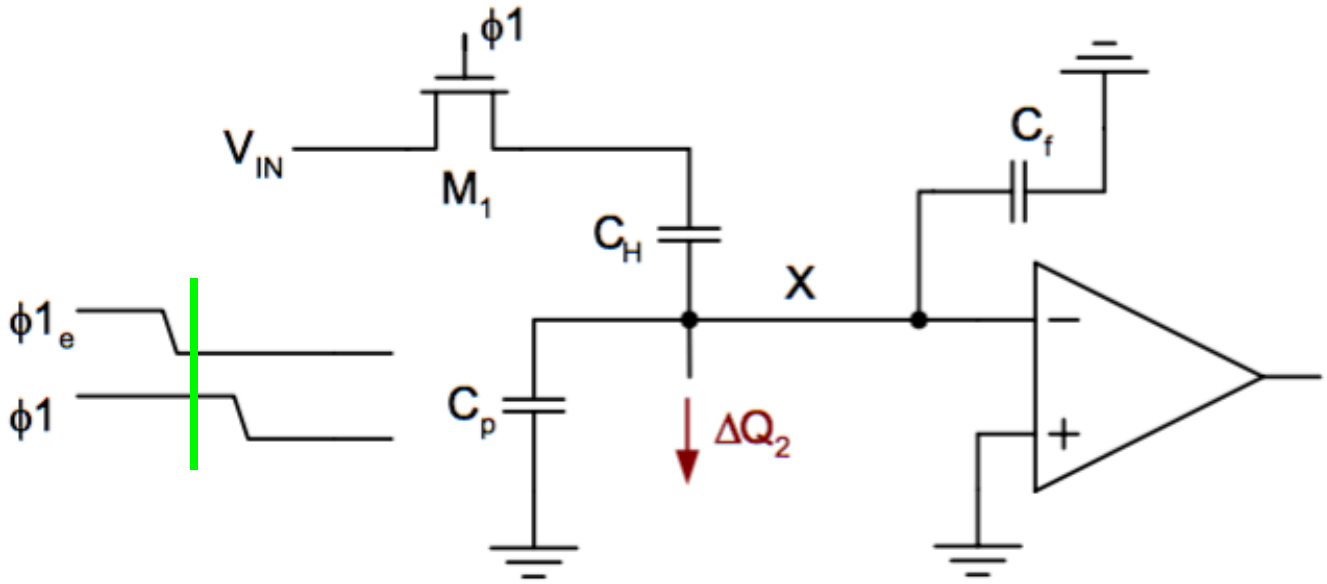


Circuit during ϕ1



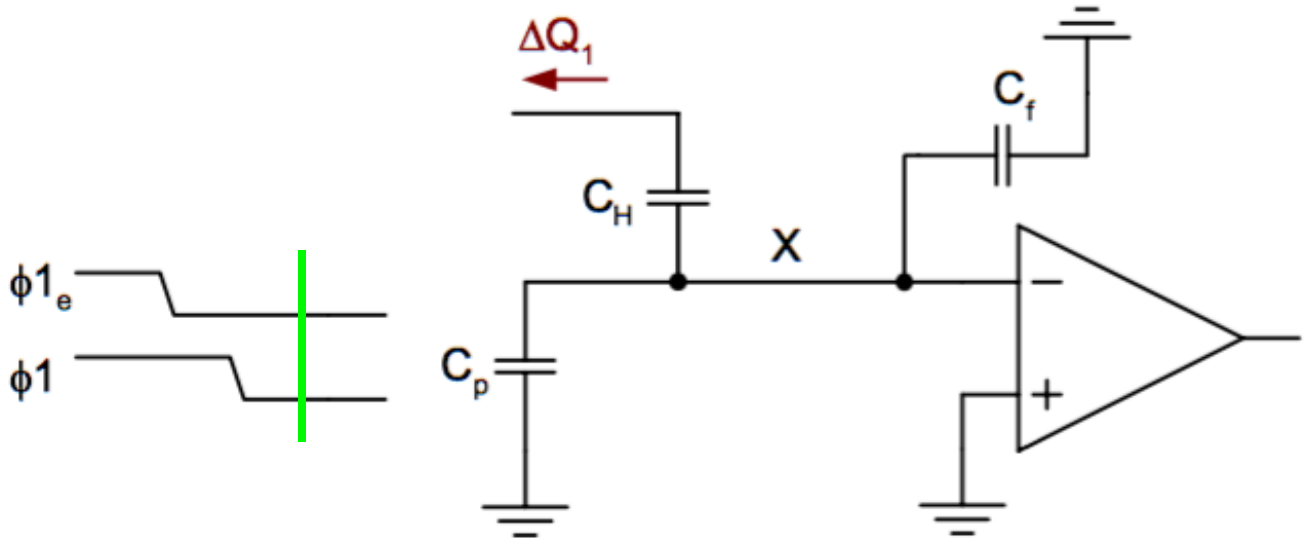
- Total charge at node X: $Q_X = -C_H V_{IN}$

Circuit during $\phi 1e$ Going Low



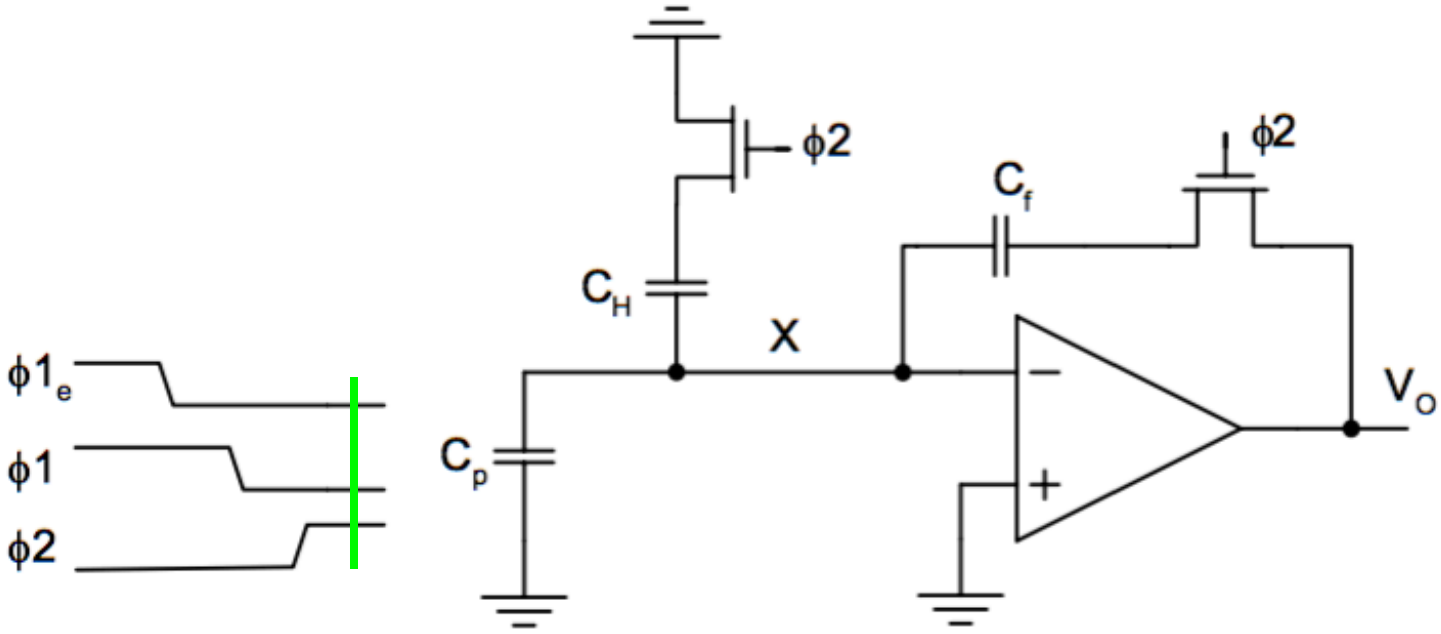
- Total charge at node X: $Q_X = -C_H V_{IN} - \Delta Q_2$

Circuit during $\phi 1$ Going Low



- Total charge at node X: $Q_X = -C_H V_{IN} - \Delta Q_2$
  - Q1 charge injection changes voltage across all caps, but total charge at X remains unchanged

Circuit during ϕ2



- Opamp forces voltage at node X to zero
  - Charge at X must redistribute among capacitors

Charge Conservation

- Sampled Charge: $Q_{X1} = -C_H V_{IN} - \Delta Q_2$
- After Redistribution: $Q_{X2} = -C_f V_O$
- Charge Conservation:

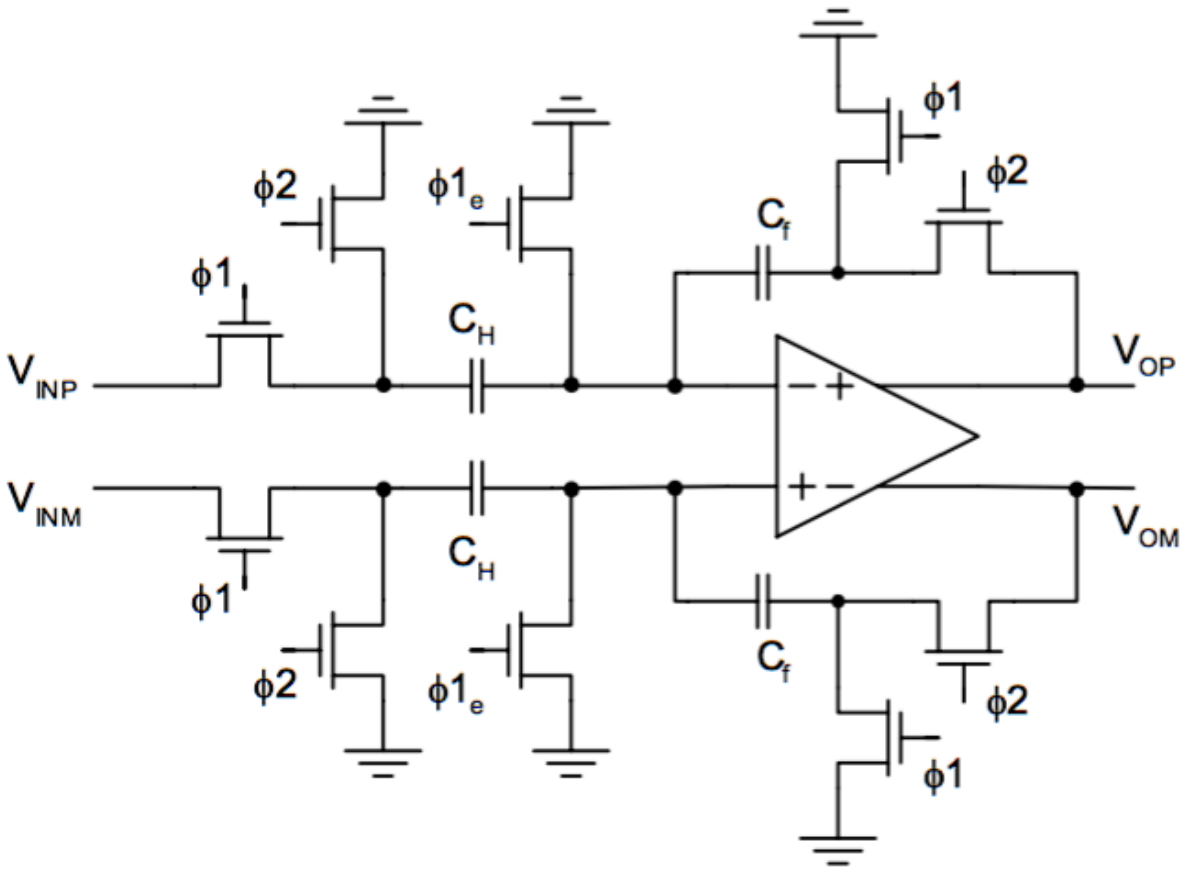
$$Q_{X1} = Q_{X2}$$

$$-C_H V_{IN} - \Delta Q_2 = -C_f V_O$$

$$\therefore V_O = \frac{C_H}{C_f} V_{IN} + \frac{\Delta Q_2}{C_f}$$

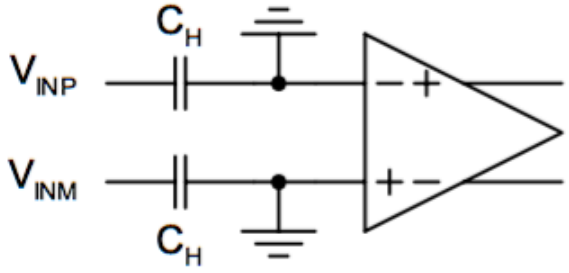
- Output has signal independent offset
  - Can easily cancel through full differential circuit

Fully Differential Circuit

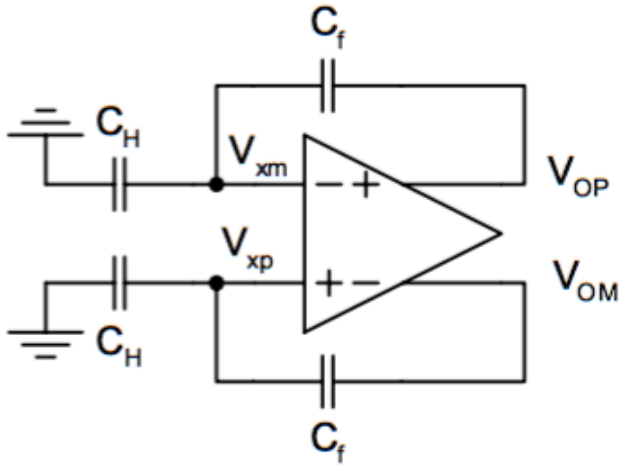


Analysis

During ϕ1



During ϕ2

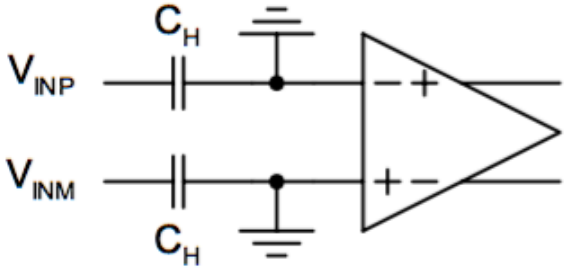


$$Q_{1m} = -C_H V_{INP} + \Delta Q \qquad Q_{2m} = C_H V_{xm} - C_f (V_{OP} - V_{xm})$$

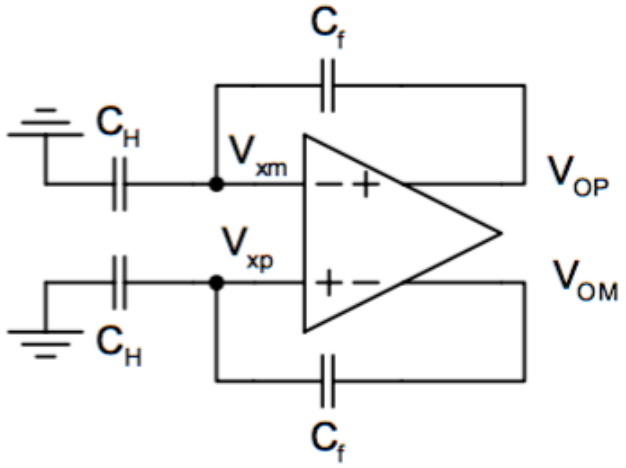
$$Q_{1p} = -C_H V_{INM} + \Delta Q \qquad Q_{2p} = C_H V_{xp} - C_f (V_{OM} - V_{xp})$$

Analysis

During ϕ1



During ϕ2



$$Q_{1m} = -C_H V_{INP} + \Delta Q \qquad Q_{2m} = C_H V_{xm} - C_f (V_{OP} - V_{xm})$$

$$Q_{1p} = -C_H V_{INM} + \Delta Q \qquad Q_{2p} = C_H V_{xp} - C_f (V_{OM} - V_{xp})$$

$$1) \quad Q_{1-} = Q_{2-}$$

$$2) \quad Q_{1+} = Q_{2+}$$

$$V_{xm} = V_{xp}$$

$$\frac{V_{OP} + V_{OM}}{2} = V_{OC}$$

Analysis

- Subtracting 1) and 2) yields

$$V_{OP} - V_{OM} = \frac{C_H}{C_f}(V_{INP} - V_{INM})$$

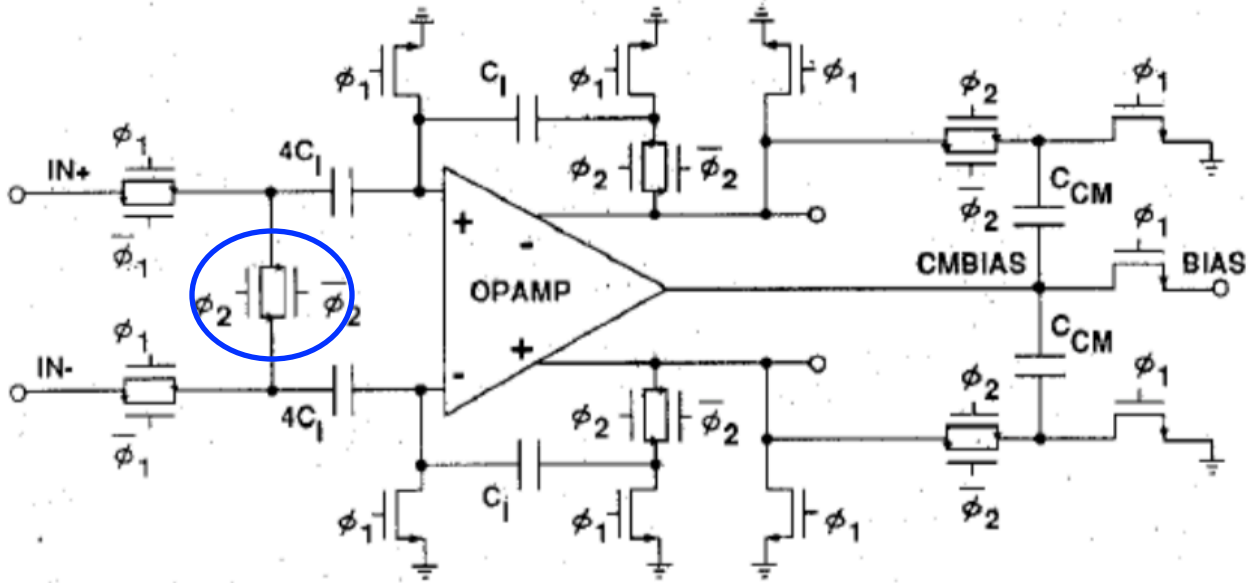
- Adding 1) and 2) yields

$$-C_H(V_{INP} + V_{INM}) + 2\Delta Q = (C_H + C_f)(V_{xp} + V_{xm}) - C_f(V_{OP} + V_{OM})$$

$$V_{xc} = \frac{\Delta Q}{C_H + C_f} + \frac{C_f}{C_H + C_f} V_{OC} - \frac{C_H}{C_H + C_f} V_{IC}$$

- Variation in V_{IC} show up as common mode variations at the amp input
  - Need good CMRR

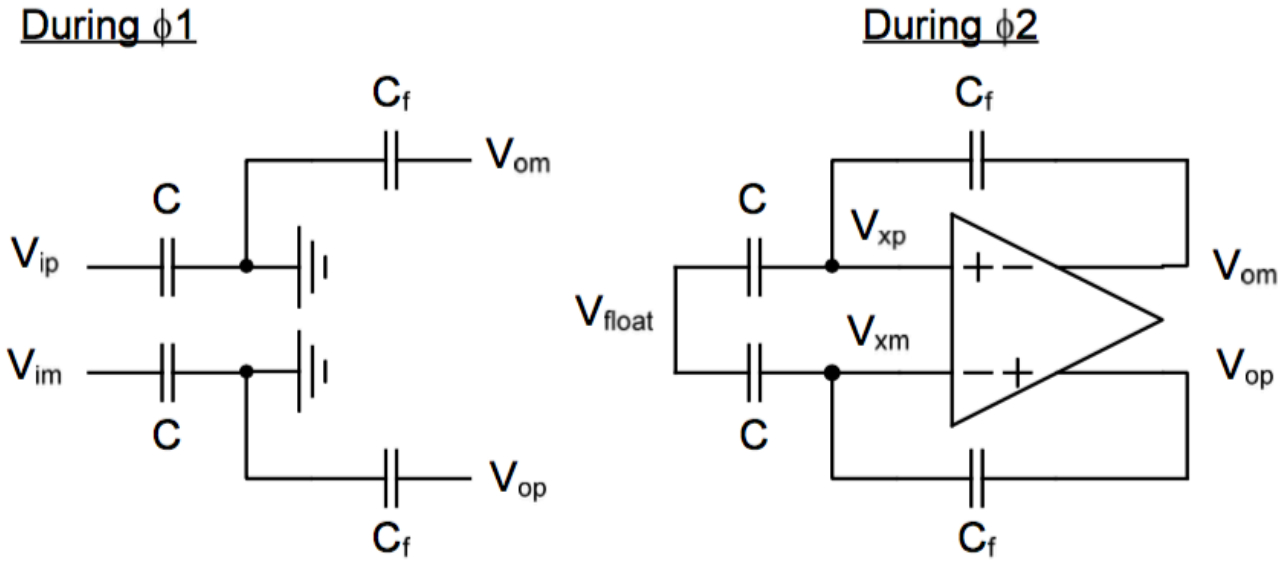
T/H with Common Mode Cancellation (Reference)



S.H. Lewis & P.R. Gray, "A Pipelined 5 MSample/s 9-bit Analog-to-Digital Converter", IEEE J. Solid-State Circuits, pp. 954-961, Dec. 1987

- Short switch allows to re-distribute only differential charge on sampling capacitors
- Common mode at OPAMP input becomes independent of common mode at circuit input terminals (IN+/IN-)

Analysis (Reference)



- Charge conservation at V_{ip}, V_{im} and V_{float}

$$\left(V_{ip}+V_{im}\right)\cdot C=\left(V_{float}-V_{xp}\right)\cdot C+\left(V_{float}-V_{xm}\right)\cdot C$$

$$V_{ic}=V_{float}-V_{xc}$$

$$V_{float}=V_{ic}+V_{xc}$$

Analysis (Reference)

- Common mode charge conservation at amplifier inputs

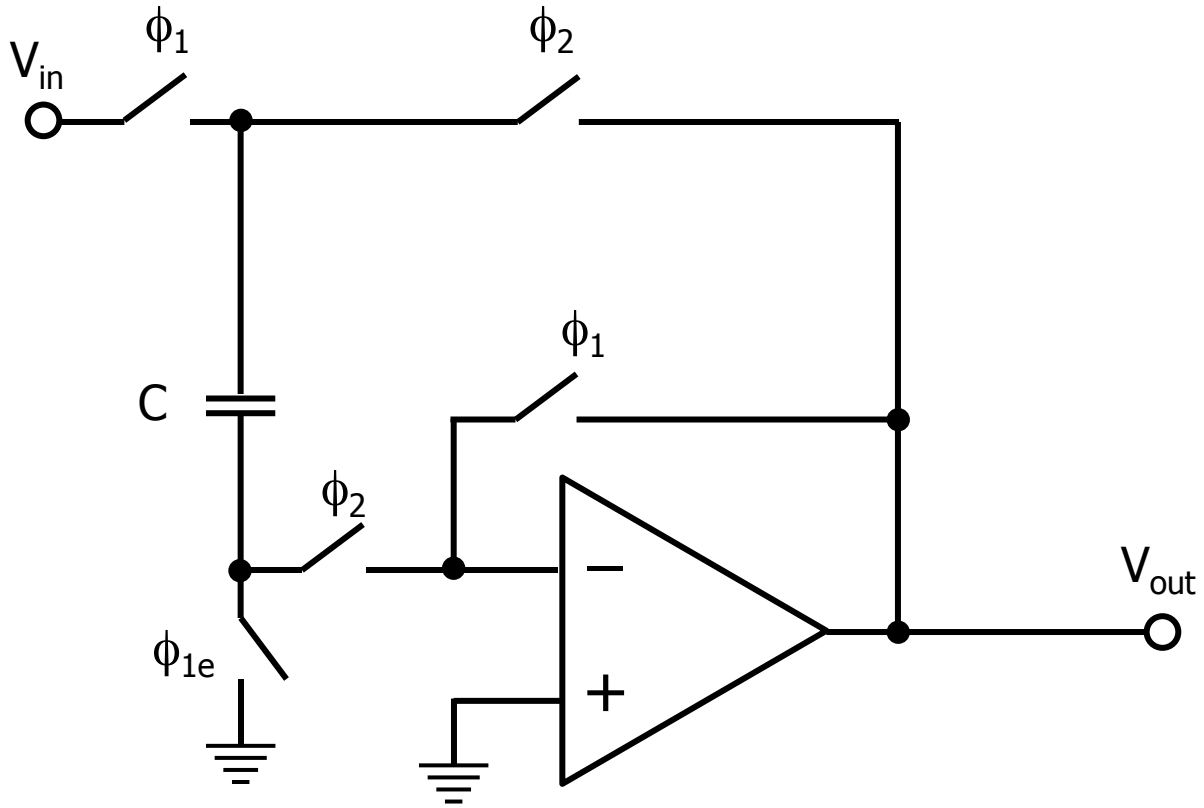
$$V_{ic} \cdot C + V_{oc} \cdot C_f = (V_{float} - V_{xc}) \cdot C + (V_{oc} - V_{xc}) \cdot C_f$$

$$V_{ic} \cdot C = ([V_{ic} + V_{xc}] - V_{xc}) \cdot C - V_{xc} \cdot C_f$$

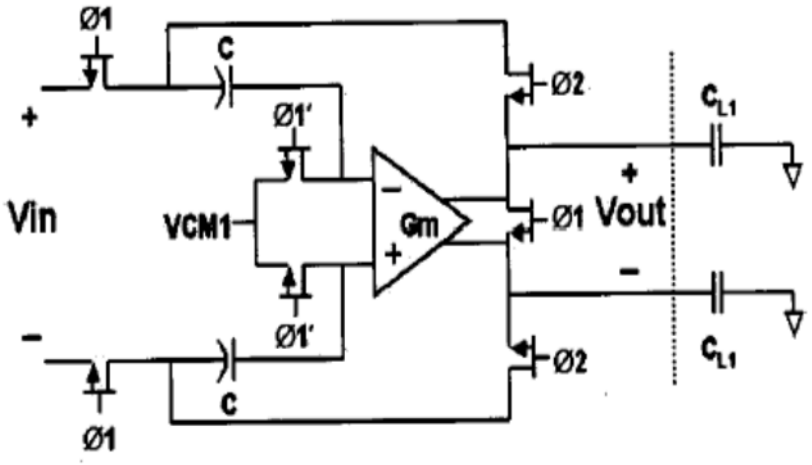
$$0 = V_{xc}$$

- Amplifier input common mode (V_{XC}) is independent of
  - Input common mode
  - Output common mode

Flip-Around Track and Hold



Flip-Around T/H

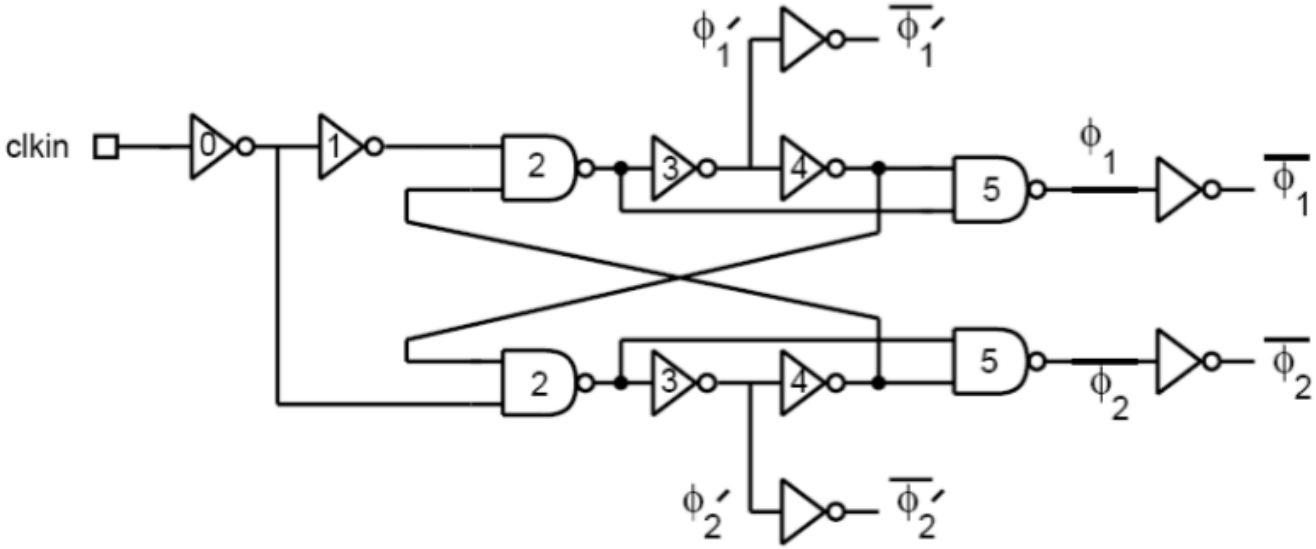


[W. Yang et al., "A 3-V 340-mW 14-b 75-MSample/s CMOS ADC With 85-dB SFDR at Nyquist Input", IEEE J. Solid-State Circuits, pp. 1931-1936, Dec. 2001]

- Sampling caps are "flipped around" and used as feedback capacitors during $\phi 2$
- Pros: improved feedback factor (lower noise, higher speed), smaller area
- Cons: Amp is subjected to input common mode variations

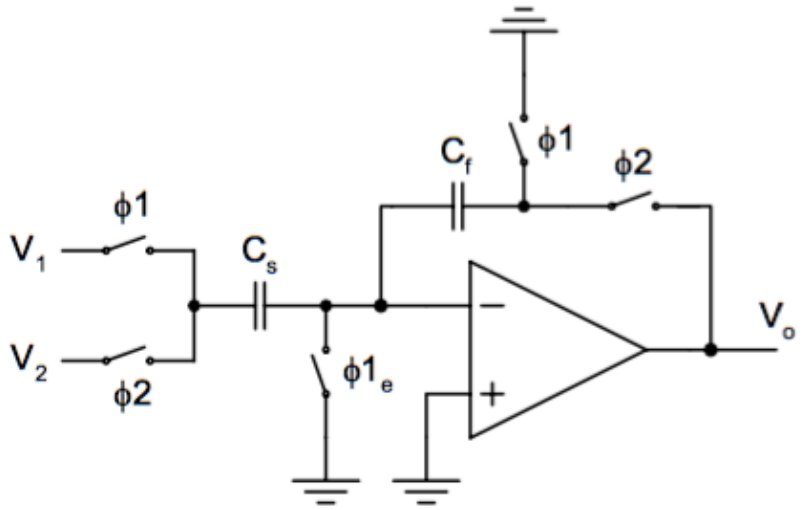
Clock Generation

- Non-overlapping clocks



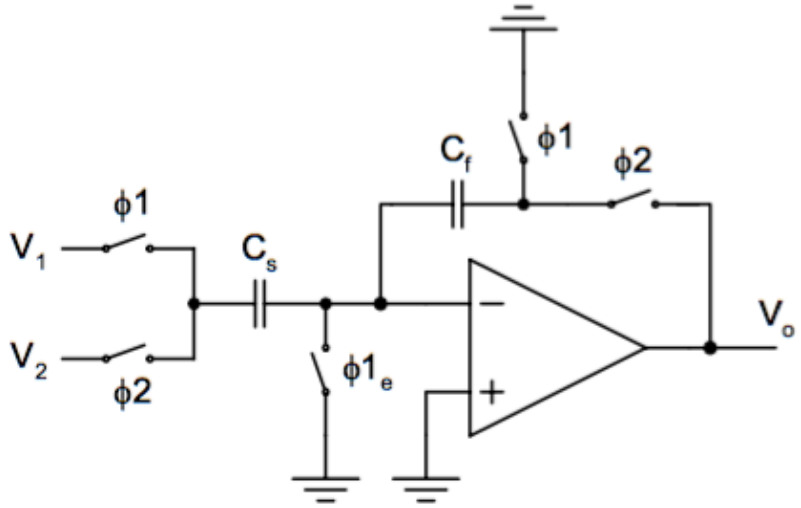
[A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," PhD Thesis, UC Berkeley, 1999]

Difference Amplifier



- Useful for computing differences of signals
  - Application example: Pipeline ADC (more later)

Difference Amplifier

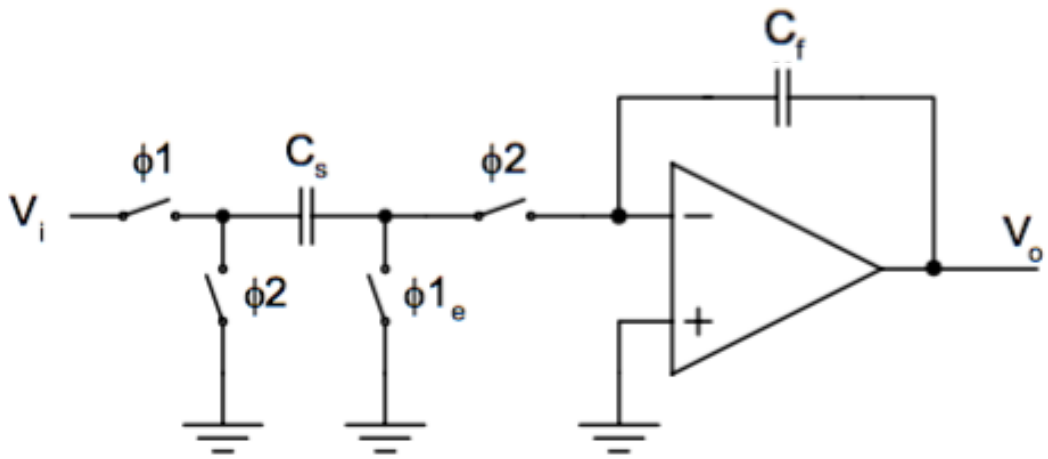


$$V_1 C_s = V_o C_f + V_2 C_s$$

$$V_o = \frac{C_s}{C_f}(V_1 - V_2)$$

- Useful for computing differences of signals
  - Application example: Pipeline ADC (more later)

Integrator



- C_f accumulates charge packets acquired during $\phi 1$
  - "Discrete time integrator"
- Used e.g. in switched capacitor sigma-delta ADCs

Big Ideas

- Elementary track-and-hold circuit
  - Many nonidealities
  - First order improvements can improve performance
- Track-and-hold topologies
  - Charge redistribution – add common mode cancellation
    - Bottom plate sampling – charge injection cancellation
    - Fully differential – eliminate signal dependent offset
  - Flip-around
    - Faster
- Clock generation – non overlapping clocks

Admin

- Proj 1
  - Due Tuesday 10/8
- HW 4
  - Due Sunday 10/13
  - ADC static and spectral metrics