ESE 570 DYNAMIC LOGIC GATES
AND CELLS
STATIC LOGIC GATES: valid logic levels are steady-state op points. Outputs are generated in response to input voltage levels after a certain time delay. Output levels are preserved as long as there is power, i.e. no refresh is needed.

DYNAMIC LOGIC GATES: valid logic level are not steady-state op points and depend on temporary storage of charge on parasitic node capacitances. Outputs are generated in response to input voltage levels and a clock. Requires periodic updating or refresh.

ADVANTAGES:
1. Allows implementation of simple sequential circuits with memory functions.
2. Use of common clock signals throughout the system enables the synchronization of various circuit blocks.
3. Implementation of complex functions generally use less die area than static circuits.
4. Often dissipates less dynamic power than static designs, due to smaller parasitic capacitances.
Comparison of Static and Dynamic Logic Implementations

Static

Pseudo-nMOS

Dynamic

Precharge → Evaluate → Precharge
Comparison of Static and Dynamic Logic Implementations

- **Static**
  - Circuit diagram showing a simple inverter with $V_{DD}$ and a single gate.

- **Pseudo-nMOS**
  - Circuit diagram showing a more complex gate with $V_{DD}$ and a ratio of 2/3.

- **Dynamic**
  - Circuit diagram showing a flipped inverter with $V_{DD}$ and a single gate.

The dynamic gate is noted as more robust compared to the static and pseudo-nMOS gates.
EXAMPLE:
Consider the following CMOS D Latch circuit:

\[ \text{CK} = 1: \text{MP turns ON.} \ C_x \text{ is charged up or down through MP depending on the input } D \text{ voltage level.} \ Q = D. \]

\[ \text{CK} = 0: \text{MP turns OFF, and} \ C_x \text{ is isolated from input } D. \ Q \text{ is determined by charge stored on } C_x \text{ during previous } \text{CK} = 1. \]
During **CK = 1**: Let $D = 1$, i.e. $V_D = V_{DD}$. MP is conducting and charges $C_x$ to a "weak 1" (i.e. $V_x = V_{DD} - V_{T0nMP}$). M1 is ON: $V_y = 0 \text{ V} < V_{T0nM3}$ => M3 is OFF: $V_Q = V_{DD} = 5 \text{ V}$ or $Q = 1$.

During **CK = 0**: Logic-level $V_x$ is preserved through charge storage on $C_x$. However, $V_x$ starts to drop due to leakage.

**WHAT IS THE MINIMUM $V_x$ NEEDED TO KEEP Q = 1 WHEN CK = 0?**
\[ V_y = V_{DD} = 5V \]

\[ \frac{k_n}{2} \left( \frac{W}{L} \right)_n \left[ 2(V_x - V_{T0n})V_y - V_y^2 \right] = \frac{k_p}{2} \left( \frac{W}{L} \right)_p \left( V_x - V_{DD} - V_{T0p} \right)^2 \]

\[ \frac{20 \mu A}{V^2} \left( 2(V_x - 1V)1V - 1V^2 \right) = \frac{10 \mu A}{V^2} \left( 4(V_x - 5V - (-1V))^2 \right) \]

\[ 2V_x * 1V - 3V^2 = (V_x - 4V)^2 \Rightarrow V_x^2 - 10VV_x + 19V^2 = 0 \]

\[ (V_x - 7.45V)(V_x - 2.55V) \]

NOTE: for \( V_Q = V_{DD} \), M3 must be OFF \( \Rightarrow V_y \leq V_{T0,M3} = 1.0 \text{ V} \);

i.e. M1 is in LIN region and M2 is OFF

Assume that \( V_y = V_{T0_n} = 1V \), i.e. just small enough to keep M3 OFF

\( \Rightarrow \) M1 LINEAR and M2 SATURATION \((V_{GD} > V_{T0_p})\)
\[ 2V_x - 1V - 3V^2 = (V_x - 4V)^2 \implies V_x^2 - 10VV_x + 19V^2 = 0 \implies \begin{align*} & (V_x - 7.45V)(V_x - 2.55V) \implies V_x = V_{x-min} = 2.55V \end{align*} \]

Therefore, \( V_x \) can drop from \( V_{x-max} = V_{DD} - V_{TMP} \) to \( V_{x-min} = 2.55 \text{ V} \) due to charge leakage before \( V_Q \) is effected (i.e. the output changes state).

\[ (W/L)^n = 2 \]
\[ (W/L)^p = 4 \]
\[ k_n' = 20 \mu A/V^2 \]
\[ k_p' = 10 \mu A/V^2 \]
\[ V_{T0n} = 1.0 \text{ V} \]
\[ V_{T0p} = -1.0 \text{ V} \]
\[ \gamma = 0.37 \text{ V}^{1/2} \]
\[ 2\phi_F = -0.6 \text{ V} \]
CK = 0: CHARGE STORAGE AND CHARGE LEAKAGE

At t = 0 CK = 0, V_x = V_{max}, V_{in} = 0 V

I_{leakage} = I_{reverse} + I_{subthreshold}

I_{leakage} = I_{reverse} + I_{subthreshold}
\[ V_{in} = 0 \]

\[ V_{CK} = 0 \]

\[ I_{leakage} = I_{subthreshold} + I_{reverse} \]

\[ C_x = C_{ext} + C_j \]

DRAIN-SUB PN JUNCTION

\[ C_{ext} = C_{gb} + C_{poly} + C_{metal} \]
\[ C_x = C_{ext} + \frac{A C_j 0}{\sqrt{1 + \frac{V_x}{\phi_0}}} + \frac{P C_j 0_{sw}}{\sqrt{1 + \frac{V_x}{\phi_{0_{sw}}}}} \]

\[ I_{leakage} = C_x \frac{dV_x}{dt} \text{ where } C_x = C_{ext} + C_j \]

FOR QUICK ESTIMATE OF WORST CASE LEAKAGE BEHAVIOR

worst case hold time \( (t_{\text{hold}}) \) -> shortest time for \( V_x \) to drop from its initial logic "1" value \( V_{x-max} \) to \( V_{x-min} \) due to leakage.

\[ \min(t_{\text{hold}}) = \Delta t = \frac{C_{x-min}}{I_{leakage-max}} \Delta V_x = \frac{C_{x-min}}{I_{leakage-max}} (V_{x-max} - V_{x-min}) \]

\[ V_{x-max} = V_{DD} - V_{Tn,MP} \text{ and } V_{x-min} = 2.55 \text{ V} \]

\[ C_{x-min} = C_{ext} + C_{j-min} \text{ where } C_{j-min} = C_j (V_x = V_{x-max}) \]
EXAMPLE 9.2
Consider the soft-node structure shown, which consists of the drain (or source depending on current direction) terminal of the pass transistor, connected to the poly gate of an nMOS driver transistor via a metal interconnect. Estimate the worst-case (min) hold time if \( V_{DD} = 5 \text{ V} \) and the soft-node is initially charged to \( V_{x-max} \). Assume that \( I_{leakage-max} = 0.85 \text{ pA} \).

\[
V_{x-max} = V_{DD} - V_{TMP} \quad V_{x-min} = 2.55 \text{ V}
\]
VT₀ = 1.0 V
γamma = 0.4 V¹/²
PHI = -0.6 V
PB = 0.88 V
PBsw = 0.95 V
XJ = 0.2 μm
Iₗeakage,max = 0.85 pA

Cₙ₋ₚ, Aₙ₋ₚ = Cₒx Aₙ₋ₚ = 0.095 fF/μm²
C₋ₚ₋ₚ, P₋ₚ₋ₚ = CJSW P₋ₚ₋ₚ = 0.200 fF/μm

Cₒx = 0.06 fF/μm²
C’ₘₐₑタル₉ = 0.036 fF/μm²
C’ₚₒₗₑ₉ = 0.055 fF/μm²
Cᵢ₀ = CJ = 0.095 fF/μm²
Cᵢ₀sw = CJSW = 0.200 fF/μm

(W/L)ₙ = 2
(W/L)ₚ = 4
k’ₙ = 20 μA/V²
k’ₚ = 10 μA/V²
Vₜ₀ₙ = 1.0 V
Vₜ₀ₚ = -1.0 V
γ = 0.37 V¹/²
2φₒ = -0.6 V

Cₒ = Cₒₓ W Lₘₐₛ₉ = 0.065 fF/μm² (4 μm x 2 μm) = 0.52 fF
Cₘₐₑタル₉ = C’ₘₐₑタル₉ W Lₘₐₑ₉ = 0.036 fF/μm² (5 μm x 5 μm) = 0.90 fF
Cₚₒₗₑ₉ = C’ₚₒₗₑ₉ W Lₚₒₗₑ₉ = 0.055 fF/μm² (36 μm² + 6 μm² + 2 μm²) = 2.42 fF
C₋ₚ₋ₚ, A₋ₚ₋ₚ = Cᵢ₀ A₋ₚ₋ₚ = 0.095 fF/μm² (36 μm² + 12 μm² + 0.8 μm²) = 4.56 fF
C₋ₚ₋ₚ, P₋ₚ₋ₚ = CJSW P₋ₚ₋ₚ = 0.200 fF/μm (18 μm + 6 μm + 2 μm) = 5.20 fF
Need $V_{x,max}$ to determine $C_{j,min}$

$$V_{x-max} = V_{DD} - V_{T,MP} = V_{DD} - VT0 - GAMMA \left( \sqrt{-PHI + V_{SB}} - \sqrt{-PHI} \right)$$

$$= 5.0 V - 1.0 V - 0.4 V^{1/2} \left( \sqrt{0.6 V + V_{x-max}} - \sqrt{0.6 V} \right)$$

$$V_{x-max} - 4.3 V = -0.4 V^{1/2} \left( \sqrt{0.6 V + V_{x-max}} \right)$$

Solving for $V_{x-max}$: $V_{x-max} = 3.68 V$

$$C_{j-min} = \frac{C_{n+p}}{\sqrt{1 + \frac{V_x}{\phi_0}}} + \frac{C_{n+p-}}{\sqrt{1 + \frac{V_x}{\phi_{0sw}}}} = \frac{4.56 \ fF}{\sqrt{1 + \frac{3.68}{0.88}}} + \frac{5.20 \ fF}{\sqrt{1 + \frac{3.68}{0.95}}} = 4.36 \ fF$$

$$C_{x,min} = C_{gb} + C_{poly} + C_{metal} + C_{j-min}$$

$$= 0.52 \ fF + 2.42 \ fF + 0.90 \ fF + 4.36 \ fF = 8.20 \ fF$$

$$\min(t_{hold}) = \frac{C_{x-min}}{I_{leakage-max}} (V_{x-max} - V_{x-min}) = \frac{8.20 \times 10^{-15} F}{0.85 \times 10^{-12} A} (3.68 V - 2.55 V) = 10.9 \ ms$$
SYNCHRONOUS DYNAMIC CIRCUIT TECHNIQUES

\[ \phi_1, \phi_2 \text{ NON-OVERLAPING CLOCKS} \]

\[ \phi_1 \rightarrow \text{phase 1} \]

\[ \phi_2 \rightarrow \text{phase 2} \]

LOGIC LEVELS DURING INACTIVE CLOCK PHASE ARE STORED ON INPUT CAPS
CONVERTING STATIC LOGIC TO DYNAMIC LOGIC
Asynchronous Combinational Static Logic

Synchronous CASCADED Dynamic Logic

Kenneth R. Laker, University of Pennsylvania, updated 25Mar15
Charge Sharing is an issue when $\phi_1$, $\phi_2$ close.

HIGH Portion of $\phi_1$, $\phi_2$ CLOCK PHASES MUST BE LONG ENOUGH: for $C_{\text{in}k}$ to charge up or down and $C_{\text{out}k}$ to charge to new value for $k = 1,2,3$.

When $V_{\text{out}(i)} = 0V$ (or 5V) and $V_{\text{in}(i+1)} = 5V$ (or 0V) for $i = 1,2$ (stage).

“Charge Sharing” is an issue when $\phi_1$, $\phi_2$ close.
\[ V_{out1} = C_{out1}V_b \text{ and } Q_{in2} = C_{in2}V_a \]

\[ Q_{total} = C_{out1}V_b + C_{in2}V_a \text{ and } C_{total} = C_{out1} + C_{in2} \]

The resulting voltage across \( C_{total} \) is

\[ V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1}V_b + C_{in2}V_a}{C_{out1} + C_{in2}} \]

If \( V_b = V_{DD} \text{ and } V_a \ll V_b \Rightarrow V_R \approx \frac{C_{out1}V_{DD}}{C_{out1} + C_{in2}} \]

\[ V_R \approx V_{DD} \text{ if } C_{out1} \gg C_{in2} \]

“Rule of Thumb” make \( C_{out1} = 10 \, C_{in2} \).
If \( V_b = 0 \) and \( V_a = V_{DD} \) \( \Rightarrow \) \( V_R \approx \frac{C_{in2} V_{DD}}{C_{out1} + C_{in2}} \)

\[ V_R \approx \frac{C_{in2}}{C_{out1}} V_{DD} \ll V_{DD} \text{ if } C_{out1} \gg C_{in2} \]

“Rule of Thumb” make \( C_{out1} = 10 C_{in2} \)
2 - STAGE SYNCRONOUS COMPLEX LOGIC CIRCUIT

\[ F_1 = (A + B) \cdot C \]

\[ F_2 = \overline{F_1 \cdot D} \]
DYNAMIC CMOS TRANSMISSION GATE LOGIC

STAGE 1

STAGE 2

A, B, C, D

F1, F2
CMOS TRANSMISSION GATE DYNAMIC SHIFT REGISTER

Diagram showing the CMOS transmission gate dynamic shift register with nodes labeled as follows:

- $V_{in}$
- $V_{out}$
- $V_{DD}$
- $C_x$
- $M1$
- $M2$
- $\phi_1$
- $\phi_2$

The diagram also highlights a "soft node" and indicates that the design is more robust.
DYNAMIC CMOS PRECHARGE – EVALUATE LOGIC

[Diagram showing CMOS precharge and evaluation logic with transistors and nodes labeled.]
DYNAMIC CMOS PRECHARGE - EVALUATE LOGIC
SIGNIFICANTLY REDUCED TRANSISTOR COUNT
(NO COMBINATIONAL LOGIC STAGES)

CK = 0 -> Z precharges to $V_{DD}$
(inputs are applied, output is unavailable during precharge)

CK = 1 -> Z is selectively discharged to 0V or remains at $V_{DD}$ (depends on logic values of inputs)
(output is only available after discharge of C is complete)

single phase P-E logic circuit
EXAMPLE

CK = 0 => Z = ?
CK = 1 => Z = ?
Z = “0” when CK = “1”
AND
 D AND E = “1”
OR  A AND B = “1”
OR  A AND C = “1”

Z = “1” when CK = “0”
independent of inputs

Z = \[ A \cdot (B + C) + D \cdot E \] when CK = 1

Z = “1” when CK = 0
ADVANTAGES AND DISADVANTAGES VS. STATIC LOGIC

ADVANTAGES ?

DISADVANTAGES ?

Image of a diagram showing a circuit with labels such as $V_{DD}$, $M_p$, $M_e$, inputs, Logic Block, and $C$-internal capacitance.
ADVANTAGES/DISADVANTAGES

1. Requires N + 2 transistors to realize an N-input gate.
2. Low static power dissipation.
3. No dc current paths to place constraints on device sizing.
4. Input capacitance same as pseudo nMOS gate.
5. Pull-up time is improved by active switch to $V_{DD}$.

1. Output is available $\leq 50\%$ of the time.
2. Pull-down time is degraded due to series active switch to 0.
3. Logic output value can be degraded due to charge sharing with other gate capacitances connected to the output.
4. Minimum clock rate determined by leakage on C.
5. Maximum clock rate determined by C discharge time and input delays.
6. Inputs can only change during the precharge phase. Inputs must be stable during evaluation; otherwise an incorrect value on an input could erroneously discharge the output node.

(single phase P-E logic gates can not be cascaded)
PROBLEM: ALL STAGES MUST EVALUATE SIMULTANEOUSLY
SINGLE CLOCK DOES NOT PERMIT PIPELINING OF STAGES
Cascaded Domino CMOS Logic Gates

inputs

CK

V_{DD}

0 -> 1

precharged to 0

nMOS-Logic Block 1

O1

evaluate

t_{eval}

CK

precharge

O1

O2

Max # stages limited: total prop delay < t_{eval}.

propagating gate decisions

O3

nMOS-Logic Block 2

O2

evaluate

t_{eval}

nMOS-Logic Block 3

O3

0 -> 1
PROBLEM: ALL STAGES MUST EVALUATE SIMULTANEOUSLY
SINGLE CLOCK DOES NOT PERMIT PIPELINING OF STAGES
Weak pull-up (small $k_p$, i.e. small $(W/L)_p$) pMOS transistor used to maintain a pre-charged high if the clock were to stop. Suitably weakened so that it does not interfere with pull-down during evaluation when the clock is operational.

Also helps prevent erroneous discharges of C due to charge sharing with node capacitors within the nMOS Logic Block.
CHARGE SHARING BETWEEN OUTPUT CAPACITANCE $C_1$ AND INTERMEDIATE NODE CAPACITANCE $C_2$ DURING EVALUATION

1. Assume initially that all inputs are 0V and voltage across $C_2$ is at 0V.
2. During pre-charge, i.e. $CK = 0$, $C_1$ is charged to $V_{DD}$.
3. If the input to N1 switches from 0 to 1 during the evaluation phase, i.e. $CK = 1$, charge initially stored on $C_1$ will be shared with $C_2$; thus, reducing the value of $V_x$.

$$V_x = \frac{V_{DD}C_1}{C_1 + C_2}$$

KEEP $C_2 << C_1$
SEPERATE pMOS TRANSISTORS TO PRECHARGE INTERMEDIATE HIGH CAPACITANCE NODES
MULTIPLE OUTPUT DOMINO LOGIC - ALLOWS SIMULTANEOUS REALIZATION OF SEVERAL FUNCTIONS

EFFECTIVELY REDUCES ALL CHARGE SHARING PROBLEMS DURING EVALUATION
Since all nodes are pre-charged there is no charge-sharing.

\[ Z_1 = G_1 + P_1 \times P_0 \]
\[ Z_2 = G_2 + P_2 \times G_1 + P_2 \times P_1 \times P_0 = G_2 + P_2 \times Z_1 \]
\[ Z_3 = G_3 + P_3 \times G_2 + P_3 \times P_2 \times G_1 + P_3 \times P_2 \times P_1 \times P_0 = G_3 + P_3 \times Z_2 \]
\[ Z_4 = G_4 + P_4 \times G_3 + P_4 \times P_3 \times G_2 + P_4 \times P_3 \times P_2 \times G_1 + P_4 \times P_3 \times P_1 \times P_0 = G_4 + P_4 \times Z_3 \]
\[ V_x = V_{DD} \text{ at } t = \text{precharge} \]

Let \( C_1 = C_2 = 0.05 \text{ pF} \)

Let \( V_{x2} = 0 \text{ at } t = \text{precharge} \)

nMOS Logic Block

\[
\begin{align*}
V_A & = 0 \\
V_B & = 0 \\
\text{CK} & = 0 \\
\text{V}_{DD} & = V_{DD}
\end{align*}
\]

WITHOUT

PRECHARGE: \( V_{x1} \neq V_{x2} \)

EVALUATION: \( V_{x1} = \frac{V_{DD}C_1}{C_1 + C_2} = \frac{V_{DD}}{2} \)

WITH

PRECHARGE: \( V_{x1} = V_{x2} \)

EVALUATION: \( V_{x1} = V_{DD} \)
NP DOMINO CMOS (NORA OR ZIPPER DOMINO) GATES

CK and \overline{CK} - sensitive to clock skew

NOTE: INVERTERS ARE NOT REQUIRED AT OUTPUTS OF STAGES

ALL inputs stable when \( CK = 1 \)
ADVANTAGES NORA VS. DOMINO CMOS
1. No Inverters, i.e. save two transistors per stage.

DISADVANTAGES NORA VS. DOMINO CMOS
1. Selective pull-up pMOS net is slow, e.g. pMOS transistors require scaling.
2. Floating dynamic outputs are susceptible to noise, i.e. no inverters to drive succeeding stages.
TRUE SINGLE PHASE CLOCK (TSPC) PIPELINED DYNAMIC CMOS

Using tristate inverters between stages decouples the stages and enables pipelined operation.

CK - LOW: nMOS Blocks Precharge to \(V_{DD}\) (N-BLOCK Inv. Tristate)
P-MOS Blocks \(V_{o2}\) evaluates by selective pull up to \(V_{DD}\) (P-BLOCK Inv. active)

CK-HIGH: pMOS Blocks Pre-discharge to 0V (P-BLOCK Inv. Tristate)
nMOS Blocks \(V_{o1}\) evaluates by selective pull down to 0V (N-BLOCK Inv. active)

Since CK-Inverse is not used, no clock skew problem can arise.
PROVIDES SIMILAR PERFORMANCE TO NORA STRUCTURE.
CK = 1

Using tristate inverters between stages decouples the stages and enables pipelined operation.
**CK = 0**

**HIGH - Z**

**INV**

**N-BLOCK**

**P-BLOCK**

Using tristate inverters between stages decouples the stages and enables pipelined operation.
SUMMARY - GUIDELINES

1. Full complementary static logic is best option in the majority of CMOS circuits. Noise-immunity not sensitive to \( k_n/k_p \); does not involve precharging of nodes; dissipates no DC power; layout can be automated. Large fan-in gates lead to complex circuit structures (2N transistors); larger parasitics; slower and higher dynamic power dissipation than alternatives; no clock and no synchronization.

2. Pseudo-nMOS static logic finds widest utility in large fan-in gates. Requires only N+1 transistors for N fan-in; smaller parasitics; faster and lower dynamic power dissipation than full COS. Noise-immunity sensitive to \( k_n/k_p \); dissipates DC power when pulled down; and not well suited for automated layout; no clock and no synchronization.

3. CMOS domino logic should be used for low-power, high speed applications. Requires N+k transistors for N fan-in, size advantages of psuedo-nMOS; dissipates no DC power; noise immunity not sensitive to \( k_n/k_p \); use of clocks enables synchronous operation. Relies on storage on soft nodes; will require thorough simulation at all the process corners to insure proper operation; some of the speed advantage over static gates is diminished by the required pre-charge (pre-discharge) time.