ESE 570 Chip Input and Output (I/O) Circuits
OVERVIEW

1. INPUT PADS – ESD PROTECTION

2. TTL-TO-CMOS LOGIC LEVEL SHIFTING

3. DIFFERENTIAL SIGNALING

4. OUTPUT PADS – L di/dt NOISE

5. BIDIRECTIONAL I/O PADS

6. ON-CHIP CLOCK GENERATION AND DISTRIBUTION

7. LATCH-UP PROTECTION IN OUTPUT PADS
ESD PROTECTION

Human Body Model (HBM)

1 MΩ
1.5 kΩ
100 pF

Simulates the touch from a charged human's finger.

Machine Model (MM)

1 MΩ

Since in MM body resistance is absent, contact with machines can be higher stress.

Charged-Device Model (CDM)

1 MΩ

Electrostatic charge builds up on a chip due to improper grounding and then discharges when a low-resistance path becomes available.

Simulates ESD phenomena of packaged ICs during manufacturing and assembly.
ATE HBM ESD and MM ESD TEST SETUP

After exposure to the ESD waveform, a failed IC exhibits latch-up or fails one or more data sheet specifications.

SPICE-generated short-circuit HBM output current waveform specified by MIL-STD 883.C/3015.7 for $C_c$ charged to 2kV.
TYPICAL ESD PROTECTED INPUT PAD

Effective protection networks can withstand up to 8 kV HBM ESD stress
or $8A \geq I \geq 2.6$ A.
INPUT PAD WITH SERIES TRANSMISSION GATE

A -> EXTERNAL (OFF-CHIP) input signal
E -> INTERNAL (ON-CHIP) enable signal
X -> INTERNAL (ON-CHIP) output signal

X = A, when E = 0
X = HIGH-IMPEDANCE STATE when E = 1

NOTE: ANY UNUSED INPUT TERMINALS SHOULD BE TIED TO V_DD OR GND USING WEAK PULL-UP OR PULL-DOWN TRANSISTORS RATHER THAN FLOAT
INVERTING INPUT PAD WITH TTL-TO-CMOS LEVEL SHIFT

V_{DD} = 5 V

x = A

LEVEL SHIFTING FROM TTL TO CMOS

V_{in} = A
V_{OH} = 2.0 V
V_{OL} = 0.8 V

CMOS
V_{out} = X
V_{OH} = V_{DD}

NM_{L} = V_{IL} - V_{OL}
NM_{H} = V_{OH} - V_{IH}

V_{OL} = 0

DESIGN FOR V_{th} = 0.8 V + (2.0 V - 0.8 V)/2 = 1.4 V
VARIATIONS IN LEVEL-SHIFT VTC DUE TO PROCESS VARIATIONS

PM-NM => nominal processing
PH-NL => strong pMOS, weak nMOS process corner
PL-NH => weak pMOS, strong nMOS process corner

IN ADDITION:
Strong (fast) nMOS, pMOS => low $V_{Tn0}$, low $V_{Top}$; high $k_n$, high $k_p$
Weak (slow) nMOS, pMOS => high $V_{Tn0}$, high $V_{Top}$; low $k_n$, low $k_p$
WORST CASE SIMULATION METHOD

Models are first partitioned into their main types, that is NMOS, PMOS, R, and C. All possible combinations of these types are then run. However, in practice, in order to reduce the number of simulation runs R and C are grouped together.

For example, if a design contained NMOS and PMOS, the following sets would be run:
1. weak nmos, weak pmos, temp.
2. weak nmos, nominal pmos, temp.
3. weak nmos, strong pmos, temp.
4. nominal nmos, weak pmos, nominal temp.
5. nominal nmos, nominal pmos, nominal temp.
6. nominal nmos, strong pmos, nominal temp.
7. strong nmos, weak pmos, high temp.
8. strong nmos, nominal pmos, high temp.
9. strong nmos, strong pmos, high temp.
A total of 9 runs.

If R and C are included, the number of runs would increase to 27.
Differential Signaling System

Transmitter

I = +i

Two-wire pair

Terminator

I = -i

Receiver

Input Pulse

Output Pulse

Noise

Noise Reduction
DIFFERENTIAL SIGNALING (LOGIC LEVELS) FOR GBPS SYSTEMS

LVPECL (low-voltage positive referenced emitter coupled logic)
LVDS (low-voltage differential signals)
HSTL (highspeed transceiver logic)
CML (current-mode logic)

Table 1.  Typical LVPECL, LVDS, HSTL, and CML Outputs

<table>
<thead>
<tr>
<th>Output</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HSTL</th>
<th>CML</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$ (Min)</td>
<td>2.275 V</td>
<td>1.400 V</td>
<td>VDDQ$^1$ - 0.4</td>
<td>$V_{CC}$$^2$</td>
</tr>
<tr>
<td>$V_{OL}$ (Max)</td>
<td>1.68 V</td>
<td>1.000 V</td>
<td>0.400 V</td>
<td>$V_{CC}$ - 0.4 V</td>
</tr>
</tbody>
</table>

Table 2.  Typical LVPECL, LVDS, CML, and HSTL Input Levels

<table>
<thead>
<tr>
<th>Input</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HSTL</th>
<th>CML</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$ (Min)</td>
<td>2.135 V</td>
<td>1.220 V</td>
<td>VRef + 0.2</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>VRef or VCM</td>
<td>2</td>
<td>1.2</td>
<td>0.75</td>
<td>$V_{CC}$ - 0.2 V</td>
</tr>
<tr>
<td>$V_{IL}$ (Max)</td>
<td>1.825 V</td>
<td>1.100 V</td>
<td>VRef -0.2</td>
<td>$V_{CC}$ - 0.4 V</td>
</tr>
<tr>
<td>$V_{ID}$ (Min)</td>
<td>310 mV</td>
<td>200 mV</td>
<td>400 mV</td>
<td>400 mV</td>
</tr>
</tbody>
</table>

$^1$ VDDQ = 1.5 V ± 10%
$^2$ $V_{CC}$ = 3.3 V ± 10%
OUTPUT PADS

TRISTABLE OUTPUT CIRCUIT

CK or ST

CK   D   P   N   Z
1    1   0   0   1 = D
1    0   1   1   0 = D
0    0   1   0   HIGH Z

Z = D for CK = 1
Z = HIGH IMP for CK = 0

LARGE W/L
-> Sufficient current sink, source
-> Reduce delay times

CK = 0 => MN2 & MP2 OFF => Z = HIGH Z
CK = 1 => MN2 & MP2 ON => Z = D
OUTPUT PADS – L $\frac{di}{dt}$ NOISE

LARGE W/L
- => Sufficient current sink, source  => LARGE $\frac{di}{dt}$
- => Reduce delay times

L ($\frac{di}{dt}$) VOLTAGE DROP ACROSS BONDING WIRE
CONNECTING PAD TO PACKAGE PIN

$I_{\text{max}} = C_{\text{load}} \left( \frac{dV_{\text{out}}}{dt} \right)_{\text{max}}$

$\approx \frac{C_{\text{load}} V_{\text{DD}}}{t_s/2}$

$\frac{I_{\text{max}}}{t_s/2}$

assume $C_{\text{load}}$ charged to $V_{\text{DD}}$

$\left[ \frac{di}{dt} \right]_{\text{max}} \geq \frac{I_{\text{max}}}{t_s/2} = \frac{2I_{\text{max}}}{t_s}$

$\geq \frac{4C_{\text{load}} V_{\text{DD}}}{(t_s)^2}$

$\approx 0.1$ to $10$ A/ns
OUTPUT PADS – L $\frac{di}{dt}$ NOISE

\[
\left[ \frac{di}{dt} \right]_{\text{max}} \geq \frac{4 C_{\text{load}} V_{\text{DD}}}{(t_s)^2}
\]

LET $C_{\text{load}} = 1$ pF, $L = 1$ nH, $V_{\text{DD}} = 3.5$ V and $t_s = 1$ ns

\[
\left[ \frac{di}{dt} \right]_{\text{max}} \geq \frac{4 \times \left( 1 \times 10^{-12} \frac{C}{V} \right) \times 3.5V}{\left( 1 \times 10^{-9} s \right)^2} = \frac{14 \times 10^{-12} A}{1 \times 10^{-9} \text{ns}} = 14 \text{ mA/}\text{ns}
\]

\[
L \left[ \frac{di}{dt} \right]_{\text{max}} \geq 14 \text{ mV}
\]

HIGH-END MICROPROCESSOR CHIPS WITH 32 BITS OR 64 BIT DATA BUS LINES - ALL OUTPUT DRIVERS SWITCHING AT THE SAME TIME!

For 32 bits switching simultaneously:

\[
32 \times L \left[ \frac{di}{dt} \right]_{\text{max}} \approx 0.45 \text{ V}
\]

PROBLEM!

REDUCE NOISE $\Rightarrow$ lower $V_{\text{DD}}$ or increase $t_s$ $\Rightarrow$ limits speed
OUTPUT PADS – REDUCE $L \frac{di}{dt}$ NOISE

PRECHARGES INVERTER OUTPUT “Z” TO $V_{DD}/2$ WHEN ST = 1 AND CK = 0 (JUST PRIOR TO CK -> 1)

ALSO, STAGGER SWITCHING TIMES OF 32 OUTPUT DRIVERS BY USING BUILT-IN DELAYS IN THE CLOCK DISTRIBUTION NET.
**DIFFERENTIAL DRIVER OUTPUT PAD**

\[ t_D = \text{Delay Element} \]

\[ A = \overline{\text{IN}} (t - t_D) \]

**IN**

**A**

**B**

**C**

**O**

**V_{DD}/2**

**2Z_0**

To a Z₀ transmission line

Much reduced \([di/dt]_{max}\)
BIDIRECTIONAL I/O PAD WITH TTL INPUT CAPABILITY

E = 1 => Z = D
E = 0 => X = high Z
E = 0 => DI = Z

TTL Level Shift

Tri-state Output

V_{DD}

E = 1 => Z = D
E = 0 => X = high Z
E = 0 => DI = Z
Clock System Architecture

- Chip receives external clock through I/O pad or an internal clock is included in the Clock Generator.

- Clock generator adjusts the global clock to the external clock.

- Global clock is distributed across the chip.

- Local drivers and “clock gaters” drive the physical clocks to clocked elements.
ON-CHIP CLOCK GENERATION AND DISTRIBUTION

SIMPLE ON-CHIP CLOCK CIRCUIT

RING OSCILLATOR

CK FREQUENCY
-\rightarrow PROCESS DEPENDENT
-\rightarrow UNSTABLE FREQUENCY

PIERCE CRYSTAL OSCILLATOR CIRCUIT

\rightarrow GOOD FREQUENCY STABILITY
TWO-PHASE CLOCK GENERATION

\[ T_c \]

\[ \text{clk} \rightarrow \text{phi}_1 \rightarrow \text{phi}_2 \]

\text{CLOCK DECODER}

\[ \text{CK1, CK2, CK3, CK4} \]

\text{PRIMARY CLOCKS FROM XTAL CONTROLLED OSCILLATOR}
Clock Skew and Jitter

• Clock should theoretically arrive simultaneously to all sequential circuits.

• Practically it arrives in different times. The differences are called *clock skews*.

• Most systems distribute a *global clock* and then use local “*clock gaters*” located near clocked elements.

• *Skews* result from paths mismatches, process variations and ambient conditions, resulting in *physical clocks ≠ global clock*. 
Clock Skew Components

**Systematic** is the portion of clock skew existing under nominal conditions. It can be minimized by appropriate design.

**Random** is variable portion of clock skew caused by random process variations like devices’ channel length, oxide thickness, threshold voltage, wire thickness, width and space. It can be measured on silicon and adjusted by DLL components.

**Drift** is time-dependent portion of clock skew caused by time-dependent environmental variations, occurring relatively slowly. Compensation of those must takes place periodically.

**Jitter** is rapid clock edge changes (deterministic and random components), occurring by power noise and clock generator jitter. It cannot be compensated.
### PLL

- **Input Clock**
- **PD**
- **LF**
- **VCO**
- **Frequency/Phase Control**
- **Output Clock**

### DLL

- **Input Clock**
- **PD**
- **LF**
- **Variable Delay Line**
- **Delay Control**
- **Output Clock**

**Clock Distribution & Buffers**
Some Representative Clock Distribution Networks

- Tree
- Mesh
- Grid
- H-Tree
- X-Tree
- Tapered H-Tree
CAD Techniques automate the generation of hierarchical clock distribution networks.
LATCH-UP IN CMOS CIRCUITS

latch-up susceptibility proportional to

\[ \frac{1}{\text{NSUB}} x \left( \frac{1}{\text{nMOS} - \text{pMOS spacing}} \right)^2 \]
LATCH-UP – POSITIVE FEEDBACK

Bipolar Current Gains
\[ \beta = \frac{I_C}{I_B} > 1 \quad 0 < \alpha = \frac{I_C}{I_E} < 1 \]
\[ \beta = \frac{\alpha}{1 - \alpha} \]

Prevent latch-up by reducing positive feedback

\[ \beta_1 \beta_2 \leq 1 \]
\[ \alpha_1 + \alpha_2 \leq 1 \]

Latch-up Analysis with
\[ R_{\text{well}} = R_{\text{sub}} = \infty \]

\[ I_{B1} = I_{C2} \]
\[ I_{B2} = I_{C1} = \beta_1 I_{B1} \]
\[ I_{C2} = \beta_2 \beta_1 I_{B1} \]

Time = \( t_1 > 0 \):
\[ I_{B1} = x \Rightarrow I_{C1} = \beta_1 x \]

Time = \( t_2 > t_1 \)
\[ I_{B2} = I_{C1} = \beta_1 x \Rightarrow I_{C2} = \beta_2 \beta_1 x \]

Positive feedback! if \( \beta_2 \beta_1 \geq 1 \)
**LATCH-UP PREVENTION**

Latch-up prevention with parasitic resistances $R_{\text{well}}$ and $R_{\text{sub}}$

$$\alpha_1 + \alpha_2 \leq 1 + \frac{R_T}{R_{\text{well}}} + \frac{R_T}{R_{\text{sub}}} \left( \frac{V_{DD}}{V_{BE}} - 2 \right)$$

Latch-up occurs if NOT satisfied

**TO PREVENT LATCH-UP:** Insure Latchup Condition is Violated!

- Reduce $\alpha_1$, $\alpha_2$
- Reduce $R_{\text{sub}}$, $R_{\text{well}}$
- Decrease $V_{DD}$

A. Use a latchup resistant process.

Latchup Prevention LAYOUT Guidelines:

B. Use $p^+$ guard rings connected to GND around nMOS transistors and $n^+$ guard rings connected to $V_{DD}$ around the pMOS transistors to reduce $R_{\text{well}}$ and $R_{\text{sub}}$ and to weaken BJTs.

C. Place sub, well contacts close to the nMOS, pMOS source connections to supply rails (i.e. GND for nMOS, $V_{DD}$ for pMOS) to reduce $R_{\text{well}}$ and $R_{\text{sub}}$.

**CONSERVATIVE RULE:** One sub contact per source connection to a supply, or GND.

**LESS CONSERVATIVE:** One sub contact per 5-10 transistors.

D. Layout nMOS, pMOS transistors close to GND, $V_{DD}$ rails, respectively and maintain space between nMOS, pMOS transistors.
OUTPUT BUFFER CELL LAYOUT WITH LATCH-UP PREVENTION

(a) No Latchup Protection

(b) Latchup Protection Using Substrate Contacts (Well taps)

(c) For I/O and other high current circuits

n+ guard ring to V_{DD}

n-well

p+ guard ring to GND

Kenneth R. Laker, University of Pennsylvania, updated 6Apr15