The Verilog Hardware Description Language

**Verilog**

**Structural**

- Gate-Level
  - Logic gates and the connections between them are described.

- Switch-Level
  - Transistors and storage nodes in a device and the connections between them are described.

**Behavioral**

- Algorithmic
  - A design algorithm is described in high-level language constructs.

- RTL
  - The flow of data between registers and the processing of that data is described. This is a state machine implementation.

You will be using structural modeling in the labs for this course. This is the simplest method, and it is the most useful for simple devices.

Recommended reading: The Verilog-XL User Guide in Openbook.

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