ESE 570: Digital Integrated Circuits and VLSI Fundamentals

Lec 17: March 23, 2017
Energy and Power Optimization, Design Space Exploration, Synchronous MOS Logic

Total Power

- $P_{\text{tot}} = P_{\text{static}} + P_{\text{sc}} + P_{\text{dyn}}$
- $P_{\text{sw}} = P_{\text{sc}} = a(C_{\text{load}}V_2f) + C_{\text{sc}}V_2f$
- $P_{\text{tot}} \approx a(C_{\text{load}}V_2f) + C_{\text{sc}}V_2f + Vt_s(W/L)e^{-V_1/(nkT/q)}$
- Let $a$ = activity factor
  $a$ = average $#\text{trans}_{\text{on}}$/clock

Energy and Power Optimization

Power Sources

- Review: $P_{\text{tot}} = P_{\text{static}} + P_{\text{dyn}} + P_{\text{sc}}$

Worksheet Problem 1

<table>
<thead>
<tr>
<th>$V_{\text{in}}$</th>
<th>$I_{\text{static}}$</th>
<th>$I_{\text{dynamic}}$</th>
<th>$I_{\text{sc}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>140mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>400mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>500mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>600mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>800mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Worksheet Problem 1

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$I_{static}$</th>
<th>$I_{dynamic}$</th>
<th>$I_{sc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>180pA</td>
<td>126uA</td>
<td></td>
</tr>
<tr>
<td>140mV</td>
<td>6nA</td>
<td>100uA</td>
<td></td>
</tr>
<tr>
<td>400mV</td>
<td>36nA</td>
<td>18uA</td>
<td></td>
</tr>
<tr>
<td>500mV</td>
<td>36nA</td>
<td>18uA</td>
<td></td>
</tr>
<tr>
<td>600mV</td>
<td>36nA</td>
<td>18uA</td>
<td></td>
</tr>
<tr>
<td>860mV</td>
<td>6nA</td>
<td>100uA</td>
<td></td>
</tr>
<tr>
<td>1V</td>
<td>180pA</td>
<td>126uA</td>
<td></td>
</tr>
</tbody>
</table>

Reminder: Worksheet Problem 1

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$I_{static}$</th>
<th>$I_{dynamic}$</th>
<th>$I_{sc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>180pA</td>
<td>126uA</td>
<td></td>
</tr>
<tr>
<td>140mV</td>
<td>6nA</td>
<td>100uA</td>
<td></td>
</tr>
<tr>
<td>400mV</td>
<td>36nA</td>
<td>18uA</td>
<td></td>
</tr>
<tr>
<td>500mV</td>
<td>36nA</td>
<td>18uA</td>
<td></td>
</tr>
<tr>
<td>600mV</td>
<td>36nA</td>
<td>18uA</td>
<td></td>
</tr>
<tr>
<td>860mV</td>
<td>6nA</td>
<td>100uA</td>
<td></td>
</tr>
<tr>
<td>1V</td>
<td>180pA</td>
<td>126uA</td>
<td></td>
</tr>
</tbody>
</table>

Reduce $V_{dd}$ (Worksheet #2)

<table>
<thead>
<tr>
<th>$V_{dd}$</th>
<th>$V_{thn}$</th>
<th>$I_{static}$</th>
<th>$I_{dynamic}$</th>
<th>$I_{sc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>520mV</td>
<td>300mV</td>
<td>0V</td>
<td>39.6uA</td>
<td></td>
</tr>
<tr>
<td>140mV</td>
<td>300mV</td>
<td>60mV</td>
<td>14.4uA</td>
<td></td>
</tr>
<tr>
<td>260mV</td>
<td>300mV</td>
<td>111nA</td>
<td>10.8uA</td>
<td></td>
</tr>
<tr>
<td>300mV</td>
<td>300mV</td>
<td>60mV</td>
<td>10.8uA</td>
<td></td>
</tr>
<tr>
<td>500mV</td>
<td>300mV</td>
<td>180pA</td>
<td>36uA</td>
<td></td>
</tr>
</tbody>
</table>
Reduce \( V_{dd} \):

- \( \tau_{gd} = Q/I = (CV)/I \)
- \( I_d = (\mu C_{OX}/2)(W/L)(V_{gs} - V_{TH})^2 \)
- \( \tau_{gd} \) impact?

\[ \tau_{gd} \propto \frac{1}{V} \]

Ignoring leakage:

\[ E \propto V^2 \]
\[ E \tau^2 \approx \text{Const} \]

Reduce \( V_{dd} \) (Worksheet #3):

\( V_{thu} = |V_{thp}| = 300 \text{mV}, V_{in} = V_{dd} \), estimate \( E \tau \)

<table>
<thead>
<tr>
<th>( V_{dd} )</th>
<th>( I_{ds} )</th>
<th>( \tau/(\tau_{gd}=1) )</th>
<th>( E_{\text{switch}}/\text{const} )</th>
<th>( E \tau )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1V</td>
<td>126uA</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>700mV</td>
<td>72uA</td>
<td>1.225</td>
<td>0.49</td>
<td>0.6</td>
</tr>
<tr>
<td>500mV</td>
<td>36uA</td>
<td>1.75</td>
<td>0.25</td>
<td>0.437</td>
</tr>
<tr>
<td>350mV</td>
<td>9uA</td>
<td>4.9</td>
<td>0.12</td>
<td>0.588</td>
</tr>
<tr>
<td>260mV</td>
<td>111nA</td>
<td>295</td>
<td>0.07</td>
<td>20.6</td>
</tr>
</tbody>
</table>

Reduce Short-Circuit Power?

\( P_{sc} = aC_{sc}V^2 f \)

\[ E = V_{dd} \times \left( I_{peak} \times \tau_s \times \left( \frac{1}{2} \right) \right) \]
Increase $V_{th}$ (Worksheet #4)

- What is impact of increasing threshold on
  - Delay?
  - Leakage?
- $V_{dd} = 1V$, $V_{in} = V_{dd}$

<table>
<thead>
<tr>
<th>$V_{in} = V_{dd}$</th>
<th>$I_{in}$</th>
<th>$I_{stat}$</th>
<th>$I_{stat}/V_{th} = 300mV$</th>
</tr>
</thead>
<tbody>
<tr>
<td>300mV</td>
<td>126μA</td>
<td>1</td>
<td>180pA</td>
</tr>
<tr>
<td>460mV</td>
<td>97μA</td>
<td>1.3</td>
<td>3.6pA</td>
</tr>
<tr>
<td>600mV</td>
<td>72μA</td>
<td>1.75</td>
<td>108fA</td>
</tr>
</tbody>
</table>

Idea

- Tradeoff
  - Speed
  - Switching energy
  - Leakage energy
- Energy-Delay tradeoff: $E \tau^2$

Design Space Exploration

Design Problem

- Function: Identify equivalence of two 32bit inputs
- Optimize: Minimize total energy
- Assumptions: Match case uncommon
  - I.e. Most of the time, the inputs won’t be matched
- Deliberately focus on Energy to complement project
  - ….but will still talk about delay

Idea: Design Space Explore

- Identify options
  - All the knobs you can turn
- Explore space systematically
- Formulate continuum where possible
  - i.e. formulate trends
Problem Solvable

- Is it feasible?
  - First, make sure we have a solution so we know our main goal is optimization

- How do we decompose the problem?

Total Power

- Static CMOS:
  - \( P_{tot} \approx a(\frac{1}{2}C_{load} + C_{sc})V^2 f + V_I (W/L) e^{V_t/(kT/q)} \)

- What can we do to reduce power?

Knobs

- What are the options and knobs we can turn?

Design Space Dimensions

- Vdd
- Topology
  - Gate choice, logical optimization
  - Fanin, fanout, Serial vs. parallel
- Gate style / logic family
  - CMOS, Ratioed (N load, P load)
- Transistor Sizing
- Vth

- The choices you make impact area, speed (delay), power

How Reduce Short-Circuit Power?

- \( P_{sc} = aC_{sc} V^2 f \)

\[
E = V_{dd} \times \left( I_{peak} \times t_{sc} \times \left( \frac{1}{2} \right) \right)
\]
Gate

- What gates might we build?
- High fanin?
- Serial-Parallel?

Logic Family

- Considerations for each logic family?
  - CMOS
  - Ratioed with PMOS load
  - Ratioed with NMOS load

Sizing

- How do we want to size gates?

Reduce Vdd

- What happens as reduce V?
  - Energy?
    - Dynamic
    - Static
  - Switching Delay?
- How low can we push Vdd?

Reduce $V_{dd}$

- $\tau_{gd} = Q/I = (CV)/I$
- $I = (\mu C_{ox}/2)(W/L)(V_{gs} - V_{TH})^2$
- $\tau_{gd}$ impact?
- $\tau_{gd} \propto 1/V$

Increase $V_{th}$?

- What is impact of increasing threshold on
  - Dynamic Energy?
  - Leakage Energy?
  - Delay?
Design Problem

- Function: Identify equivalence of two 32-bit inputs
- Optimize: Minimize total energy
- Assumptions: Match case uncommon
  - i.e. Most of the time, the inputs won’t be matched
- Deliberately focus on Energy to complement project
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Design Space Dimensions

- Vdd
- Topology
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- Gate style / logic family
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- Transistor Sizing
- Vth
- The choices you make impact area, speed (delay), power

Ideas

- Three components of power
  - \( P_{tot} = P_{static} + P_{dyn} + P_{sc} \)
- We know many things we can do to our circuits
- Design space is large
- Systematically identify dimensions
- Identify continuum (trends) tuning when possible
- Watch tradeoffs
  - ...don’t over-tune

Classes of Logic Circuits

- **COMBINATIONAL** (non-sequential)
  - BISTABLE
  - MONOSTABLE
  - ASTABLE
  - Two stable op. pts.
  - Latch – level triggered
  - Flip-Flop – edge triggered

- **SEQUENTIAL** (combinational)
  - One stable op. pt.
  - One-shot – single pulse output
  - Ring Oscillator

Sequential Circuits or State Machines:
- a. Current Output(s) depend on Current Inputs and Past Inputs via States.
- b. Suited to problems that are solved by completing several steps using current inputs and past outputs in a specific order or a sequential manner.

Functions Using Sequential Operations

- Combinational Operations
- Sequential Operations
- Arithmetic Logic Unit
- Microprocessor

- may use memory cells such as
- Flip-Flop

- to accomplish
- Binary Counter
- Decade Counter
- Frequency Counter

- which is a component of
- Microcomputer

- or
- Serial
- Parallel

- using a
- Shift Register
- Frequency Counter

- in the case of a
- Microcomputer
Sequential Circuit (or State Machine) Construct

- Register is used to Store Past Values of State(s) and Output(s)
- Synchronous Sequential Circuit – clock, outputs change with clock event
- Asynchronous Sequential Circuit – no clock, outputs change after inputs change

Static Bistable Sequential Circuits

Basic Cross-coupled Inverter pair

\[ V_{OH} = V_{DD} \]

\[ V_{OL} = 0 \]

STATIC: \( V_{DD} \) and GND are required to maintain a stable state.

Basic Bistable Cross-coupled Inverter Pair has no means to apply input(s) to change the circuit's State.

Basic Sequential Circuits (Cells)

- Latches
- Registers
Latch

- Level-sensitive device
- Positive Latch
  - Output follows input if CLK high
- Negative Latch
  - Output follows input if CLK low

\[ Q = \text{CLK} \cdot Q + \text{CLK} \cdot I_n \]

Register

- Edge-triggered storage element
- Positive edge-triggered
  - Input sampled on rising CLK edge
- Negative edge-triggered
  - Input sampled on falling CLK edge

Shift Register

- How do you make a shift register out of latches?

Two Phase Non-Overlapping Clocks

- Build master-slave register from pair of latches
- Control with non-overlapping clocks
Two Phase Non-Overlapping Clocks

- What could go wrong if the overlap?

Clocking Discipline

- Follow discipline of combinational logic broken by registers
- Compute
  - From state elements
  - Through combinational logic
  - To new values for state elements
- As long as clock cycle long enough,
  - Will get correct behavior

CMOS SR Latch – NOR2

- Operation
  - 0 0: Q', 0, Q = hold
  - 1 0: 0, Q' = set
  - 0 1: 0, Q' = reset
  - 1 1: * not allowed

CMOS SR Latch – NOR2

- SET OP:
  - S = 1, R = 0

- RESET STATE:
  - S', R = 0

- HOLD:
  - S = 0, R'

- Basic cross-coupled inverter pair

- Let at t = 0: Q', 0, Q = 1
  - At t = 1, 0 =
    - 1: S' = V, M1 ON, M4 OFF
    - 2: S = 0, 0 = M3 OFF, M3 ON
    - 5: Q' = V, M2 ON, M2 OFF
    - 4: Q, Q' = 1, 0

- Basic cross-coupled inverter pair
CMOS SR Latch – NOR2

**RESET OP:**
\[ R = 1, \ S = 0 \]

At \( t = 0 \):
1. \( Q_0 = 1, \ Q_1 = 0 \)
2. \( Q_0 = 1 \) \( \Rightarrow \ Q_0 = 0 \)
3. \( Q_0 = V_{DD}, \ Q_1 = V_{SS} \Rightarrow Q_1 = 0 \)

**HOLD OP:**
\[ S = 0, \ R = 0 \]

At \( t > 0 \):
1. \( S = 0 \) \( \Rightarrow \ Q_0 = V_{SS}, \ Q_1 = V_{DD} \)
2. \( Q_0 = Q_1 = V_{SS} \Rightarrow Q_1 = 0 \)
3. \( Q_0 = Q_1 = V_{DD} \Rightarrow Q_1 = 0 \)

Kenneth R. Laker, University of Pennsylvania, updated 25Mar15

CMOS SR Latch – NAND2

**HOLD OP:**
\[ S = 0, \ R = 0 \]

At \( t > 0 \):
1. \( S = 0 \) \( \Rightarrow \ Q_0 = V_{SS}, \ Q_1 = V_{DD} \)
2. \( Q_0 = Q_1 = V_{SS} \Rightarrow Q_1 = 0 \)
3. \( Q_0 = Q_1 = V_{DD} \Rightarrow Q_1 = 0 \)

**“ACTIVE LOW”**

<table>
<thead>
<tr>
<th>( S )</th>
<th>( R )</th>
<th>( Q_{out} )</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>*</td>
<td>hold</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>reset</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>*</td>
<td>set</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>*</td>
<td>not allowed</td>
</tr>
</tbody>
</table>

Penn ESE 570 Spring 2017 – Khanna
**Synchronous Latches**

**CLOCKED SR LATCH:** Synchronization is introduced through clock CK.

**NAND SR LATCH**

**NOTE:** S and R are asynchronous.

**CK**

**S**

**R**

**Q**

**Q'**

**WHEN** **CK** = 0, S, R **HAVE NO INFLUENCE OF** Q, Q' **=> HOLD**

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**Synchronous Latches**

**HOLD STATE:** CK = 0, S = x, R = x => Q_{n+1} = Q_n, Q_{n+1} = Q_n

**RESET STATE:** CK = 1, S = 0, R = 1 => Q_{n+1} = 0, Q_{n+1} = 1

**HOLD STATE:** CK = 1, S = 0, R = 0

**S**

**R**

**Q**

**Glitch Free Q**

**WHEN** “GLITCH” ON S (OR R) **OCCURS DURING** CK = 1, Q IS SET (OR RESET)

**LEVEL SENSITIVE:** WHEN CK = 1, ANY CHANGES IN S, R WILL EFFECT Q

---

**Latch**

- **Level-sensitive device**
- **Positive Latch**
  - Output follows input if CLK high
- **Negative Latch**
  - Output follows input if CLK low

**Positive Latch**

**Negative Latch**

---

**Static CMOS D-Latch**

**H** **CK** = 1

**D**

**CK**

**Q**

**Q'**

**D** **CK** = 1, Q_{n+1} = Q_n

**18 Transistors**

**NOT ALLOWED:**

**NO TOGGLE**

**NO NOT ALLOWED INPUTS**

---

**Kenneth R. Laker, University of Pennsylvania, updated 25Mar15**

---

**Static CMOS D-Latch**

**H** **CK** = 1

**D**

**CK**

**Q**

**Q'**

**D** **CK** = 0, Q_{n+1} = Q_n

**18 Transistors**

**NOT ALLOWED:**

**NO TOGGLE**

**NO NOT ALLOWED INPUTS**
**Transistor level implementation using transmission gates requires fewer transistors.**

When CK = 1, output Q = D, and tracks D until CK = 0, the D-Latch is referred to as positive level triggered.

When CK → 1 to 0, the Q = D is captured, held (or stored) in the Latch.

**Ideas**

- Synchronize circuits to external events (e.g., Clk)
- disciplined reuse of circuitry
- Leads to clocked circuit discipline
- Uses state holding element (e.g., Latches and registers)
- Prevents timing assumptions
- (More) complex reasoning about all possible timings

**Admin**

- HW 6 due 3/28 @ midnight