ESE 570: Digital Integrated Circuits and VLSI Fundamentals

Lec 2: January 22, 2019

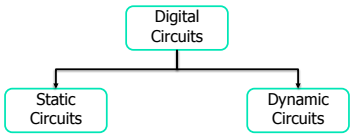
MOS Fabrication pt. 1: Physics and Methodology

Lecture Outline

- Digital CMOS Basics
- VLSI Fundamentals
- Fabrication Process

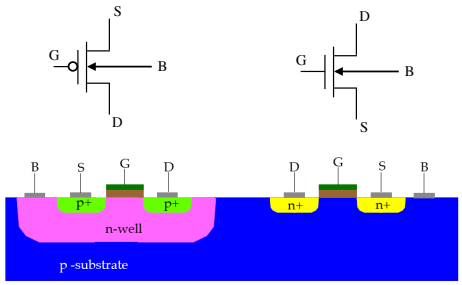
Digital CMOS Basics

Classification of Digital CMOS Circuits

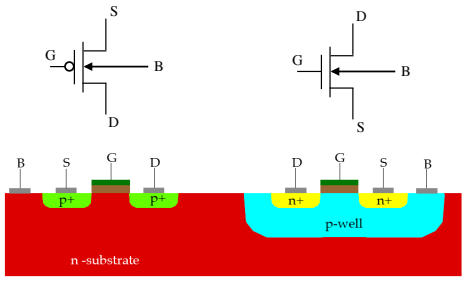


- Static Circuit
  - In steady-state the output is evaluated via a low-impedance path between the output and VDD or GND, respectively. I.e the output is actively driven.
- Dynamic Circuit
  - In steady-state the output is evaluated due to the presence or absence of charge, respectively, stored on the output node capacitance.

MOS Transistors



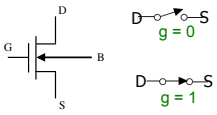
MOS Transistors



Ideal nMOS and pMOS Characteristics

SYMBOLS SWITCH CHARACTERISTICS

N- SWITCH



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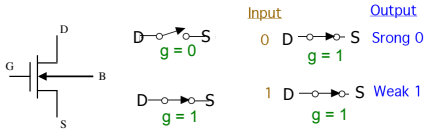
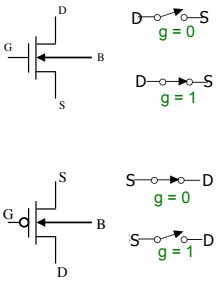


Ideal nMOS and pMOS Characteristics

SYMBOLS SWITCH CHARACTERISTICS

N- SWITCH

P- SWITCH



Ideal nMOS and pMOS Characteristics

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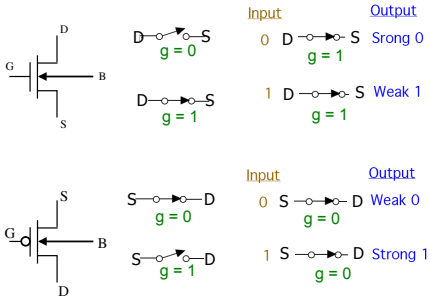
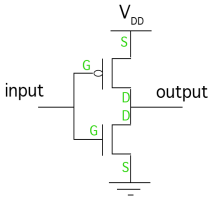


Ideal CMOS Inverter

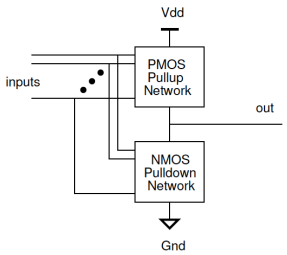


Inverter Truth Table

INPUT	OUTPUT
0	1
1	0

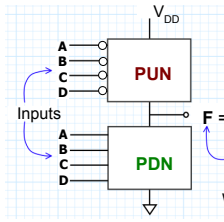
Inverter Symbol

CMOS Gates



- Complementary Metal Oxide Semiconductor

CMOS Gates



When the **PUN** is conducting, the output **F** will be "1". Hence,the **PUN** is determined by a Boolean expression for the un-complemented output **F** in terms of the complemented inputs **($\bar{A}$,$\bar{B}$,$\bar{C}$,$\bar{D}$).**

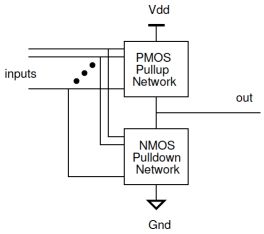
F = f(A,B,C,D)

Output

When the **PDN** is conducting, the output **F** will be "0". Hence,the **PDN** is determined by a Boolean expression for the complemented output **F** in terms of the un-complemented inputs **(A,B,C,D)**.

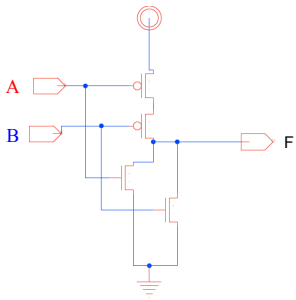
PUN and **PDN** are Dual Networks

Static CMOS Source/Drains

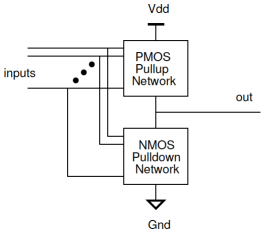


- With PMOS on top, NMOS on bottom
  - PMOS source always at top (near V_{dd})
  - NMOS source always at bottom (near Gnd)
  - Why not use NMOS for pullup network?

What gate is this?

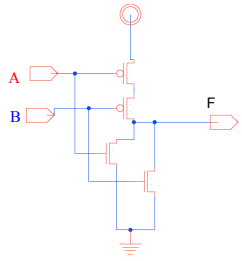


Static CMOS Gate Structure



- Drives rail-to-rail
  - Power rails are V_{dd} and Gnd
  - output is V_{dd} or Gnd
- Input connects to gates → load is capacitive
- Once output node is charged doesn't use energy (no static current —only leakage)
- Output actively driven

Two-Input CMOS NOR Gate

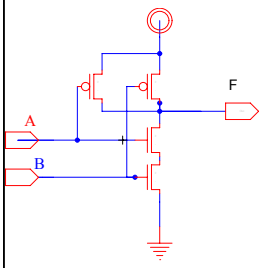


2-INPUT CMOS NOR GATE TRUTH TABLE

OUTPUT	A-INPUT 0	A-INPUT 1
B-INPUT 0	0^U 1 Z^D	Z^U 0 0^D
B-INPUT 1	Z^U 0 0^D	Z^U 0 0^D

0 = Low Impedance (short circuit)
Z = High Impedance (open circuit)

Two-Input CMOS NAND Gate



2-INPUT CMOS NAND GATE TRUTH TABLE

OUTPUT	A-INPUT 0	A-INPUT 1
B-INPUT 0		
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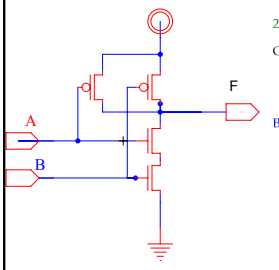
Two-Input CMOS NAND Gate



2-INPUT CMOS NAND GATE TRUTH TABLE

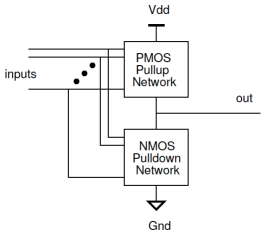
OUTPUT / B-INPUT \ A-INPUT	0	1
0	$0^U\ 1_{Z^D}$	$0^U\ 1_{Z^D}$
1	$0^U\ 1_{Z^D}$	$Z^U\ 0_{0^D}$

0 = Low Impedance (short circuit)
Z = High Impedance (open circuit)

Gate Design Example

- Design gate to perform: $f = (\bar{a} + \bar{b}) \cdot \bar{c}$

- Strategy:
  1. Use static CMOS structure
  2. Design PMOS pullup for f
  3. Use DeMorgan's Law to determine f'
  4. Design NMOS pulldown for f'



Gate Design Example

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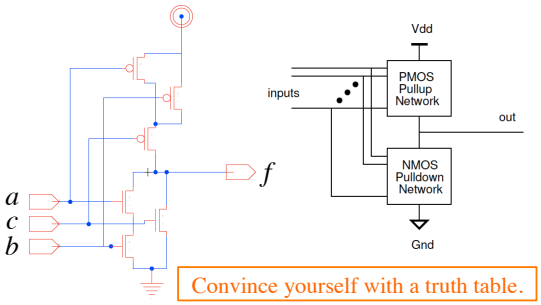


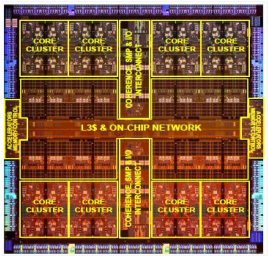
Convince yourself with a truth table.

Constructing Compound CMOS Gates

$$F = \overline{(A \cdot B + C \cdot D)}$$

VLSI Fundamentals

Oracle SPARC M7 Processor



VLSI Hierarchical Representations

- Complex digital systems can be sub-divided in a hierarchical manner
- Highly automated techniques exist for converting high level descriptions of system behaviour to a detailed implementation prescription to fabricate a chip
- To do this, a set of abstractions and domains have been developed to describe integrated electronic systems

Design Domains

- Designs are represented in three domains
  - Behavioral – What does the system do?
  - Structural – How are the elements connected?
  - Physical – How is the structure to be fabricated?

Design Abstractions

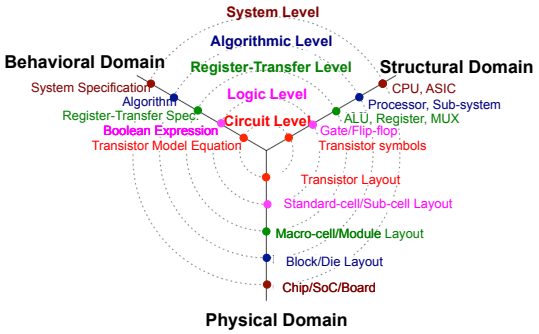
- Each domain can be specified at a variety of levels of abstraction
  - Architectural
  - Algorithmic
  - Module or Functional Block
  - Logical
  - Switch
  - Circuit

Higher Level

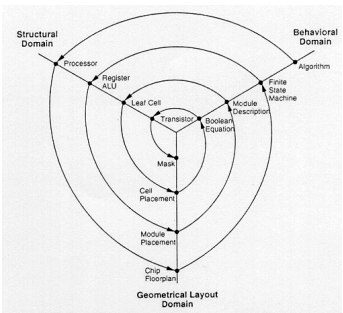
↓

Lower Level

Y-Chart: Abstractions in three Domains



Y-Chart: Abstractions in three Domains



Goal of All VLSI Design Enterprises

- Convert system specs into an IC design in MINIMUM TIME and with MAXIMUM LIKLIHOOD that the Design will PEFORM AS SPECIFIED when fabricated.

- MAX YIELD + MIN DEVELOPMENT TIME + MIN DIE AREA=> MIN COST

Fabrication Details

Silicon Ingot and Wafer Manufacturing

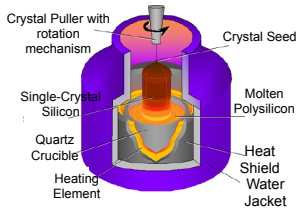
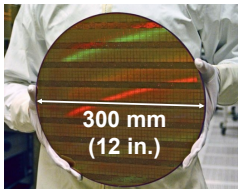


Image from Quirk & Serda

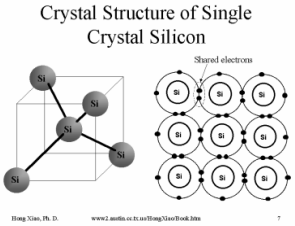
Silicon Wafer Manufacturing

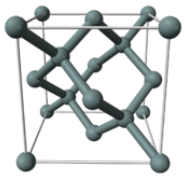


- The ROI of 450mm wafers is compelling:
  - A 450mm fab with equal wafer capacity to a 300mm fab can produce 2x the amount of die.
  - A 14nm die from a 450mm wafer will cost 23% less than the same die from a 300mm wafer.

Silicon Lattice

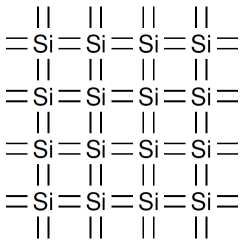
- Forms into crystal lattice





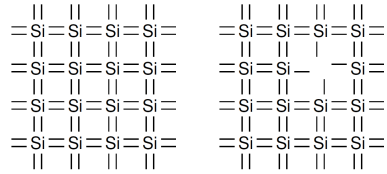
Silicon Lattice

- Cartoon two-dimensional view

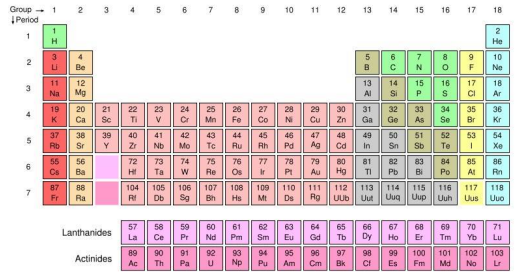


Doping

- Add impurities to Silicon Lattice
  - Replace a Si atom at a lattice site with another



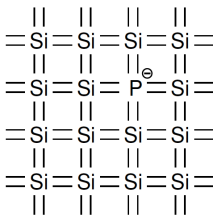
Doping Elements



http://chemistry.about.com/od/imagesclipartstructures/ig/Science-Pictures/Periodic-Table-of-the-Elements.htm

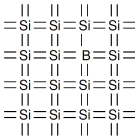
Doping with P (N-type)

- End up with extra electrons
  - Donor electrons
- Not tightly bound to atom
  - Low energy to displace
  - Easy for these electrons to move

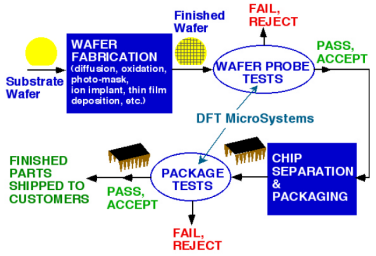


Doping with B (P-type)

- End up with electron vacancies -- Holes
  - Acceptor electron sites
- Easy for electrons to shift into these sites
  - Low energy to displace
  - Easy for the electrons to move
    - Movement of an electron best viewed as movement of hole



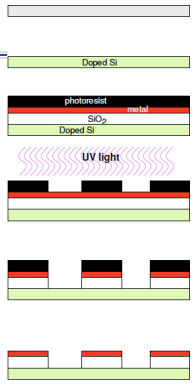
IC Manufacturing Steps



Fabrication involves many repetitions of four basic steps
- Photolithography: transfer mask patterns to the chip
- Diffusion or Ion Implantation: selective doping of Si
- Oxidation: SiO_2 growth
- Deposition: Al, polysilicon and Si_3N_4 (silicon nitride) thin films

Fabrication

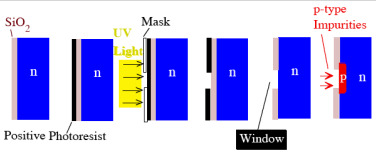
- Start with Silicon wafer
- Dope
- Grow Oxide (SiO_2)
- Deposit Metal
- Mask/Etch to define where features go



https://youtu.be/35jWSQXku74?t=121

Time Code: 2:00-4:30

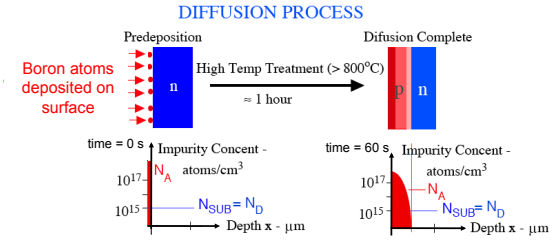
Photolithography



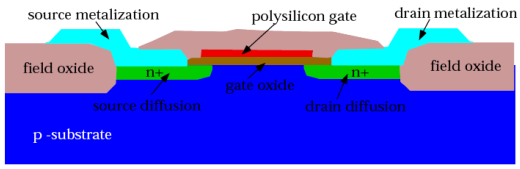
- Positive Photoresist -> exposed photoresist becomes soluble to certain chemicals.
- Negative Photoresist -> exposed photoresist becomes insoluble to certain chemicals.
- Positive Photoresist has higher resolution than Negative Photoresist

Methods of Inserting Impurity Atoms into Si Substrate
- Diffusion (impurity applied at Si surface, high temperature and long time, control of doping concentration not very precise)
- Ion implantation (impurity applied by scanning a high energy focussed ion beam at Si surface, low temperature, high acceleration, precise control of doping concentration)

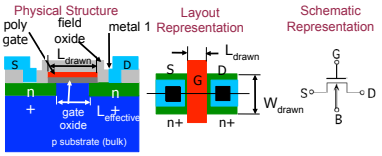
CMOS Processing Technology



Fabricated n-MOS Transistor



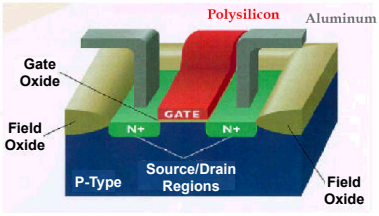
n-MOS Transistor Representations



NMOS physical structure:
- p-substrate
- n+ source/drain
- gate oxide (SiO_2)
- polysilicon gate
- CVD oxide
- metal 1
- $L_{eff} < L_{drawn}$ (lateral doping effects)

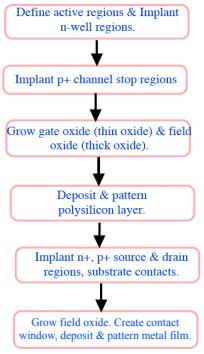
NMOS layout representation:
- Implicit layers:
  - oxide layers
  - substrate (bulk)
- Drawn layers:
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers

nMOS Transistor from a 3D Perspective

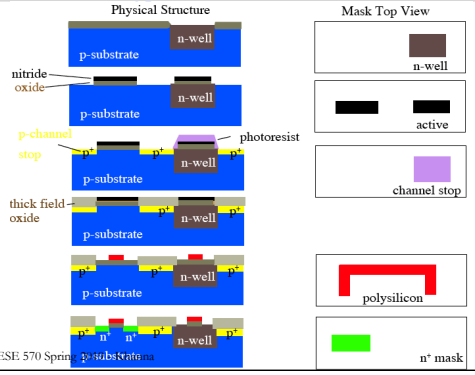


Fabrication Process

Simplified process sequence for the fabrication of an n-well CMOS IC (p substrate) with a single polysilicon layer and single metal layer



Typical N-Well CMOS Process



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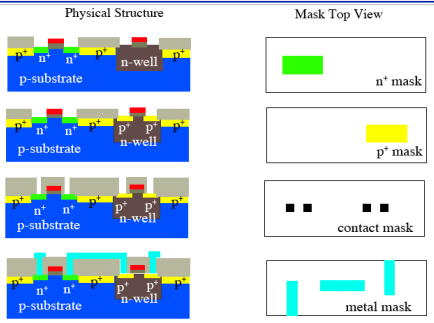
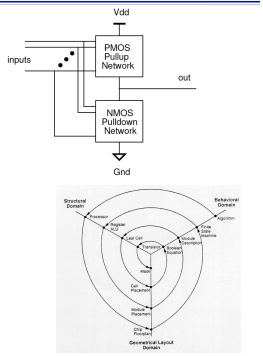


Big Idea

- Systematic construction of any gate from transistors with CMOS PUN and PDN
- Hierarchical design process in three domains (behavioural, structural, and physical) allows for complicated designs motivated cost as a function of performance, yield and design time



Admin

- New classroom: Towne 311
- Behind the scenes programming note:
  - Additional grader: Yifeng Zhang
- Enroll in Piazza site
  - piazza.com/upenn/spring2019/ese570
- Homework 1 due Friday
  - Journal articles may show up in lecture…