Phase Change Memory
An Architecture and Systems Perspective

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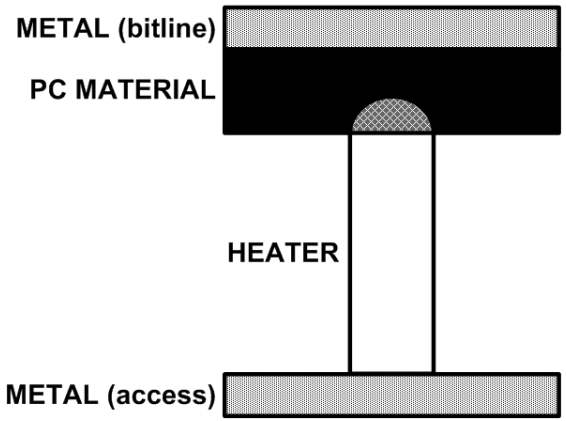
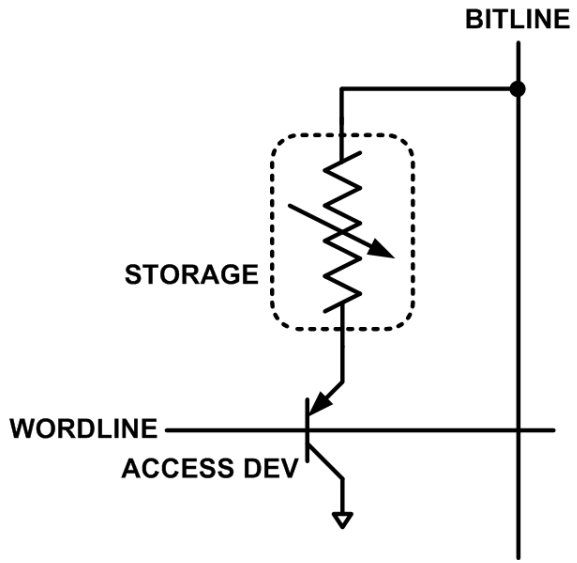
Technology Challenges

- **Memory Scaling**
  - $\Uparrow$ density, capacity; $\Downarrow$ cost
  - Challenges for prevalent technologies
- **Charge Memory**
  - Write data by capturing charge Q
  - Read data by detecting voltage V
  - Examples: Flash, DRAM
- **Resistive Memory**
  - Write data by pulsing current dQ/dt
  - Read data by detecting resistance R
  - Examples: PCM, MRAM, memristors

Phase Change Memory

- Store data within phase change material [Ovshinsky68]
- Set phase via current pulse (amorphous/crystalline)
- Detect phase via resistance





Scalability and Architecture [1]

- **PCM Scalability**
  - Scale programming current with device size [Raoux+08]
  - Lower dynamic power with scalable memory
  - Lower static power with resistive memory
- **PCM on Memory Bus**
  - Exploit low latencies, byte-addressability
  - Explore buffer design, wear reduction/leveling
- **PCM as DRAM Alternative**
  - 1.5x size, 4-12x latency, 2-43x energy
  - 1.2x app delay, 1.0x mem energy, >5-year lifetime

[1] B.Lee et al. **"Architecting phase change memory as a scalable DRAM alternative."** ISCA-36: International Symposium on Computer Architecture 2009.

Non-Volatility and Systems [2]

- **PCM File System**
  - Improve consistency with COW, atomicity, ordering
  - Improve safety with persistence in O(ms) not O(s)
  - Improve performance over NTFS on RAM
- **Architectural Support**
  - Atomic 8B writes with capacitive support
  - Ordered writes with barrier-delimited epochs
- **Applied Non-Volatility**
  - Instant start/hibernate
  - Inexpensive checkpointing

[2] J.Condit et al. **"Better I/O through byte-addressable, persistent memory."** SOSP-22: Symposium on Operating System Principles 2009.

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