

## **Advanced Computer Architecture I**

### **ECE 252 / CPS 220**

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#### **Meeting Time & Location**

TuTh 1:15 – 2:30PM  
Teer 203

#### **Teaching Team**

Professor Benjamin Lee  
Office: 210 Hudson Hall  
Office Hours: TuTh 530-630PM  
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Teaching Assistant: Marisabel Guevara  
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#### **Webpage**

[http://www.duke.edu/~BCL15/class\\_ece252fall11.html](http://www.duke.edu/~BCL15/class_ece252fall11.html)

#### **Synopsis**

This course covers fundamental aspects of advanced computer architecture design and analysis. Topics include processor design, superscalar and out-of-order execution, caches and memory hierarchies, virtual memory, storage systems, simulation techniques, technology trends, and future challenges. Students will complete a collaborative research project.

After completing this course, students should be able to

- Understand modern processor architectures.
- Define and evaluate design metrics.
- Define and execute a research project.

Final project and paper required. Appropriate for graduate students, as well as advanced undergraduate students.

#### **Prerequisites**

Computer Science 104 or Electrical and Computer Engineering 152 or equivalent.

#### **Grading**

Homework: 30%  
Midterm Exam: 15%  
Final Exam: 25%  
Project/Paper: 30%

#### **Academic Policy**

University policy as codified by the Duke Undergraduate Honor Code will be strictly enforced. Zero tolerance for cheating and/or plagiarism.

#### **Late Policy**

Late homework (except with Dean's excuses) will be penalized by 50% if less than a day late and receive zero credit if more than a day late. No late projects will be accepted.

## Schedule

	Topic	Hennessy & Patterson
30 Aug 1 Sep	Introduction Early machines	1 B
6 Sep 8 Sep	Microcoding CISC to RISC <u>Homework #1 Due</u>	
13 Sep 15 Sep	Paper discussion I Pipelining I	A.1-A.3
20 Sep 22 Sep	Pipelining II Instruction-level parallelism I	A.4 A.5-A.8
27 Sep 29 Sep	Instruction-level parallelism II Instruction-level parallelism III <u>Homework #2 Due</u>	2 3.1-3.4
4 Oct 6 Oct	Paper discussion II Midterm exam	
11 Oct 13 Oct	Fall break Memory I	C.1-C.3
18 Oct 20 Oct	Memory II Virtual memory <u>Homework #3 Due</u>	C.4-C.8
25 Oct 27 Oct	Paper discussion III VLIW	G
1 Nov 3 Nov	Vectors Multi-threading	F 3.5-3.9
8 Nov 10 Nov	Multiprocessors <u>Homework #4 Due</u> Paper discussion IV	4
15 Nov 17 Nov	Advanced topics – technology Advanced topics – specialization	
22 Nov 24 Nov	Advanced topics – datacenters Thanksgiving	
29 Nov 1 Dec	Paper discussion IV <u>Homework #5 Due</u> Summary	

## Research Readings

<b>Paper Discussion I</b>	<ul style="list-style-type: none"><li>• Hill et al. "Classic machines: Technology, implementation, and economics"</li><li>• Moore. "Cramming more components onto integrated circuits"</li><li>• Radin. "The 801 minicomputer"</li><li>• Patterson et al. "The case for the Reduced Instruction Set Computer"</li><li>• Colwell et al. "Instruction sets and beyond: Computers, complexity, controversy"</li></ul>
<b>Paper Discussion II</b>	<ul style="list-style-type: none"><li>• Srinivasan et al. "Optimizing pipelines for power and performance"</li><li>• Mahlke et al. "A Comparison of Full and Partial Predicated Execution Support for ILP Processors"</li><li>• Palacharla et al. "Complexity-Effective Superscalar Processors"</li><li>• Yeh et al. "Two-Level Adaptive Training Branch Prediction"</li></ul>
<b>Paper Discussion III</b>	<ul style="list-style-type: none"><li>• Jouppi. "Improving direct-mapped cache performance by the addition of a small fully-associative cache and prefetch buffers"</li><li>• Kim et al. "An adaptive, non-uniform cache structure for wire-delay dominated on-chip caches"</li><li>• Fromm et al. "The Energy Efficiency of IRAM Architectures"</li><li>• Lee et al. "Phase change memory architecture and the quest for scalability"</li></ul>
<b>Paper Discussion IV</b>	<ul style="list-style-type: none"><li>• Mudge, "Power: A first-class architectural design constraint"</li><li>• Lamport. "How to make a multiprocessor computer that correctly executes multiprocess programs"</li><li>• Lenoski et al. "The Stanford DASH Multiprocessor"</li><li>• Tullsen et al. "Simultaneous multithreading: Maximizing on-chip parallelism"</li></ul>
<b>Paper Discussion V</b>	<ul style="list-style-type: none"><li>• Horowitz et al. "Scaling, power, and the future of CMOS"</li><li>• Reddi et al. "Web search using mobile cores: Quantifying and mitigating the price of efficiency"</li><li>• Dally et al. "Efficient Embedded Computing"</li></ul>