Duke ECE 496 – Spring 2013 – Project Part 2: Memory 25 Points. Due electronically by 11:59pm on January 25th.

In this part of the project, you will implement the instruction and data memories that you will use in your processor. <u>This assignment is the *only* exception to the rule about not using Quartus megafunctions – memories must be implemented through megafunctions on the FPGA</u>. You will use Quartus' Megafunction Wizard to create the two memories. Before proceeding, make sure that you are using Quartus II Web Edition 9.1 Service Pack 2, as the Megafunction Wizard can differ substantially from release to release.

Since the architecture for your processor uses separate instruction and data memory spaces, your microarchitecture should have separate instruction and data memory blocks.

Project Part 2a: Instruction Memory

To make the instruction memory (imem.vhd), start by going to Tools ➡MegaWizard Plug-In Manager. On Page 1, select "Create" and click Next.

MegaWizard Plug-In Manager [page 1]			
*	The MegaWizard Plug-In Manager helps you create or modify design files that contain custom variations of megafunctions.		
	Which action do you want to perform?		
Â	 Create a new custom megafunction variation Edit an existing custom megafunction variation Copy an existing custom megafunction variation 		
	Copyright (C) 1991-2009 Altera Corporation		
Cancel < Back Next > Finish			

On Page 2a, select "Cyclone II" as the device family, select "VHDL" as the output file type, and set the output file name to "imem.vhd" in your working directory. On the left side, select "Installed Plug-Ins" • "Memory Compiler" • "ROM: 1-PORT". Then click Next.

MegaWizard Plug-In Manager [page 2a]	×
Which megafunction would you like to customize? Select a megafunction from the list below Installed Plug-Ins Altera SOPC Builder Altera SOPC Builder Altera SOPC Builder Communications Gates JOSP JOSP JOSP JOSP JOSP JOSP JOSP	Which device family will you be using? Which type of output file do you want to create? AHDL YHDL Verilog HDL What name do you want for the gutput file? Browse Isers\jsi3\Documents\# ECE 152 TA\Project 2 - Memory\imem.vhd
Homerraces JTAG-accessible Extensions JTAG-accessible Extensions ALTOTP ALTOT	 Return to this page for another create operation Note: To compile a project successfully in the Quartus II software, your design files must be in the project directory, in the global user libraries specified in the Options dialog box (Tools menu), or a user library specified in the User Libraries page of the Settings dialog box (Assignments menu). Your current user library directories are:
IP MegaStore	Cancel < <u>B</u> ack <u>N</u> ext > <u>Finish</u>

On Page 3, set the output bus width to 32 bits, set the memory size to 4096 words, set the memory block type to "M4K", set the block depth to "Auto", and set the clocking method to "Single clock". Then click Next.

MegaWizard Plug-In Manager - ROM: 1-PORT [page 3 of 7]			
ROM: 1-PORT	<u>A</u> bout <u>D</u> ocumentation		
1 Parameter 2 EDA 3 Summary Settings			
General Regs/Clkens/Adrs Mem Init	Currently selected device family: Cyclone II		
address[110]	Match project/default		
Clock Block type: M4K	How wide should the 'q' output bus be? 32 v bits How many 32-bit words of memory? 4096 v words		
	What should the memory block type be? ○ Auto ○ M512		
	O M-RAM O LCs Options Set the maximum block depth to Auto words		
	What clocking method would you like to use?		
Resource Usage 32 M4K	O Dual clock: use separate 'input' and 'output' clocks		
	Cancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish		

On Page 4, uncheck the register on the output port and check the clock enable. Then click Next.

MegaWizard Plug-In Manager - ROM: 1-PORT [p	bage 4 of 7]		
ROM: 1-PORT		About	Documentation
1 Parameter 2 EDA 3 Summary Settings General Regs/Clkens/Adrs Mem Init			
imem address[110] grow clock clken Block type: M4K	 Which ports should be reg idata' input port idata' input port iddress' input port iq' output port iCreate one dock enable dock signal. All registere controlled by the enable Create a byte enable po What is the width of a byte Create an 'adr' asynchro for the registered ports 	istered? signal for each ed ports are signal(s). rt for byte enable? mous dear	More Options 8 v bits More Options
Resource Usage 32 M4K	Cancel	< <u>B</u> ack	Next > Einish

On Page 5, you select the Memory Initialization File (.mif) to load initial values into the memory with. A Memory Initialization File is available for you to download at http://people.ee.duke.edu/~sorin/ece152/project/testGiveMeN.imem.mif. Download, browse to, and select this file on your computer, then click Next.



On Page 6, click Next.

MegaWizard Plug-In Manager - ROM: 1-PORT [p	аде б of 7]	EDA 🗖 🗖 🗙
ROM: 1-PORT		About Documentation
1 Parameter Settings 2 EDA 3 Summary		
imem 	Simulation L To properly file(s) are no	braries simulate the generated design files, the following simulation model eeded
	File	Description
33 ptt	altera_mf	Altera megafunction simulation library
Block type: M4K		
	Timing and r	esource estimation
	Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party synthesis tool, using a timing and resource estimation netlist can allow for better design optimization. Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information.	
	Note: Netlis design and generation	t generation can be a time-intensive process. The size of the the speed of your system affect the time it takes for netlist to complete.
Resource Usage	Generat	e netlist
32 M4K		Cancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish

MegaWizard Plug-In Manager - ROM: 1-PORT [page 7 of 7] Summary			
ROM: 1-PORT		About Documentation	
1 Parameter Settings 2 EDA 3 Summary			
imem address[110] guo guo clock Block type: M4K	Turn on the files you wish to gen automatically generated, and a r Finish to generate the selected fi subsequent MegaWizard Plug-In The MegaWizard Plug-In Manage directory: C:\Users\jsi3\Documents\# ECE	erate. A gray checkmark indicates a file that is ed checkmark indicates an optional file. Click iles. The state of each checkbox is maintained in Manager sessions. er creates the selected files in the following 152 TA\Project 4 - Memory\	
	File	Description	
	🗹 imem.vhd	Variation file	
	imem.inc	AHDL Include file	
	imem.cmp	VHDL component declaration file	
	imem.bsf	Quartus II symbol file	
	imem_inst.vhd	Instantiation template file	
	imem_waveforms.html	Sample waveforms in summary	
	imem_wave*.jpg	Sample waveform file(s)	
Resource Usage 32 M4K			
		Cancel < <u>B</u> ack <u>N</u> ext > <u>Finish</u>	

On Page 7, uncheck everything but the "imem.vhd" file, then click Finish.

Your instruction memory is now created. Click Yes to automatically add the memory to your project, or click No to manually add just the .vhd file to your project later.

Project Part 2b: Data Memory

To make the data memory (dmem.vhd), start by going to Tools MegaWizard Plug-In Manager. On Page 1, select "Create" and click Next.



On Page 2a, select "Cyclone II" as the device family, select "VHDL" as the output file type, and set the output file name to "dmem.vhd" in your working directory. On the left side, select "Installed Plug-Ins" • "Memory Compiler" • "RAM: 1-PORT". Then click Next.

MegaWizard Plug-In Manager [page 2a]	×
Which megafunction would you like to customize? Select a megafunction from the list below	Which device family will you be Using? Which type of output file do you want to create? AHDL VHDL Verilog HDL
Gates I/0 Gates JTAG-accessible Extensions Gates JTAG-accessible Extensions Gates JTAG-accessible Extensions Gates JTAG-accessible Extensions JT	What name do you want for the <u>o</u> utput file? Bro <u>w</u> se sers\jsi3\Documents\# ECE 152 TA\Project 2 - Memory\dmem.vhd
	Return to this page for another create operation Note: To compile a project successfully in the Quartus II software, your design files must be in the project directory, in the global user libraries specified in the Options dialog box (Tools menu), or a user library specified in the User Libraries page of the Settings dialog box (Assignments menu). Your current user library directories are:
	Cancel < <u>B</u> ack <u>N</u> ext > <u>Finish</u>

On Page 3, set the output bus width to 32 bits, set the memory size to 4096 words, set the memory block type to "M4K", set the block depth to "Auto", and set the clocking method to "Single clock". Then click Next.

MegaWizard Plug-In Manager - RAM: 1-PORT [page 3 of 7]			
RAM	<u>A</u> bout <u>D</u> ocumentation		
1 Parameter 2 EDA 3 Summary Settings			
Widths/Blk Type/Clks Regs/Clken/Byte Enable	e/Adrs > Mem Init >		
dmem	Currently selected device family: Cydone II		
data[310] wren address[110] # # # # # # # # # # # # # # # # # # #	Match project/default		
, clock	How wide should the 'q' output bus be? 32 💙 bits		
Block type: M4K	How many 32-bit words of memory? 4096 🗸 words		
What should the memory block type be?			
	○ Auto ○ M512 ○ M4K		
	O M-RAM O LCs Options		
	Set the maximum block depth to Auto words		
	What clocking method would you like to use?		
Resource Usage	O Dual clock: use separate 'input' and 'output' clocks		
32 M4K	Cancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish		

On Page 4, uncheck the register on the output port. Then click Next.

MegaWizard Plug-In Manager - RAM: 1-PORT [page 4 of 7]
RAM Parameter Settings 2 EDA 3 Summary	<u>About</u> <u>D</u> ocumentation
Widths/Bik Type/Clks Regs/Clken/Byte Enable	Mem Init Which ports should be registered? Image: data and 'wren' input Image: data and 'wren'wren' input Image: da
Resource Usage 32 M4K	Cancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish

On Page 5, you select the Memory Initialization File (.mif) to load initial values into the memory with. A Memory Initialization File is available for you to download at http://people.ee.duke.edu/~sorin/ece152/project/testGiveMeN.dmem.mif. Download, browse to, and select this file on your computer, then click Next.



On Page 6, click Next.

MegaWizard Plug-In Manager - RAM: 1-PORT [;	oage 6 of 7] E	
		<u>About</u> <u>D</u> ocumentation
1 Parameter 2 EDA 3 Summary Settings		
dmem 	Simulation Lib To properly s file(s) are new	oraries imulate the generated design files, the following simulation model eded
	File	Description
	altera_mf	Altera megafunction simulation library
Blook type: M4K		
	Timing and re	source estimation
	Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party synthesis tool, using a timing and resource estimation netlist can allow for better design optimization. Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information. Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist generation to complete.	
Resource Usage	Generate	netlist
32 M4K		Cancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish

MegaWizard Plug-In Manager - RAM: 1-PORT [page 7 of 7] Summary			
RAM		<u>A</u> bout <u>D</u> ocumentation	
1 Parameter 2 EDA 3 Summary Settings			
dmem data[310] q[310] wren address[110] gtdx star clock Block type: M4K	Turn on the files you wish to ge automatically generated, and a Finish to generate the selected subsequent MegaWizard Plug-I The MegaWizard Plug-In Manag directory: C:\Users\jsi3\Documents\# ECt	enerate. A gray checkmark indicates a file that is a red checkmark indicates an optional file. Click files. The state of each checkbox is maintained in in Manager sessions. ger creates the selected files in the following E 152 TA\Project 4 - Memory\	
Resource Usage	File Image: display d	Description Variation file AHDL Include file VHDL component declaration file Quartus II symbol file Instantiation template file Sample waveforms in summary Sample waveform file(s)	
32 M4K		Cancel < <u>B</u> ack <u>N</u> ext > <u>Finish</u>	

On Page 7, uncheck everything but the "dmem.vhd" file, then click Finish.

Your data memory is now created. Click Yes to automatically add the memory to your project, or click No to manually add just the .vhd file to your project later.

Project Part 2c: Initializing the Memories

To change the Memory Initialization File for your memories, open the imem.vhd or dmem.vhd file and go to line 89 or 94, respectively, and rename the "init_file" path to the new file.

```
81
 82
      BEGIN
 83
               <= sub wire0(31 DOWNTO 0);
          q
 84
 85
          altsyncram component : altsyncram
          GENERIC MAP (
 86
    clock enable input a => "BYPASS",
 87
               clock enable output a => "BYPASS"
 88
               init file => "testGiveMeN.imem.mif"
 89
               intended device ramily => "Cyclone if",
 90
               lpm hint => "ENABLE RUNTIME MOD=NO",
 91
               lpm type => "altsyncram",
 92
 93
               numwords a => 4096,
 94
               operation mode => "ROM",
               outdata aclr a => "NONE",
 95
               outdata reg a => "UNREGISTERED",
 96
 97
               ram block type => "M4K",
 98
               widthad a => 12,
 99
               width a => 32,
               width byteena a => 1
100
101
         )
102 E PORT MAP (
103
               clock0 => clock,
104
               address a => address,
105
               q a => sub wire0
106
          );
107
```

After implementing your memories, you should test them thoroughly to verify that they work correctly. One test waveform is provided for your instruction memory at http://people.ee.duke.edu/~sorin/ece152/project/test_imem.vwf and for your data memory at http://people.ee.duke.edu/~sorin/ece152/project/test_imem.vwf and for your data memory at http://people.ee.duke.edu/~sorin/ece152/project/test_imem.vwf and for your data memory at http://people.ee.duke.edu/~sorin/ece152/project/test_imem.vwf In addition, this assignment will be graded by running additional tests that are not provided, so do not assume that you can ignore bugs that do not manifest themselves on the one test that is provided.

Submitting This Assignment

To submit this assignment, create a Quartus Archive (Project Archive Project) named project2.qar of all the files needed to implement your design. Make sure that your top-level files are named imem.vhd and dmem.vhd. Submit the archive on the assignment page in Sakai, with the net IDs of the group members. There should be only one submission per group.